DAQ M Series

M Series User Manual

NI 622x, NI 625x, and NI 628x Devices

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December 2007
371022J-01

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National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 683 0100

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Depending on where it is operated, this Class A product could be subject to restrictions in the FCC rules. (In Canada, the Department of Communications (DOC), of Industry Canada, regulates wireless interference in much the same way.) Digital electronics emit weak signals during normal operation that can affect radio, television, or other wireless products.

All Class A products display a simple warning statement of one paragraph in length regarding interference and undesired operation. The FCC rules have restrictions regarding the locations where FCC Class A products can be operated.

Consult the FCC Web site at `www.fcc.gov` for more information.

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Federal Communications Commission

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user is required to correct the interference at their own expense.

Canadian Department of Communications

This Class A digital apparatus meets all requirements of the Canadian Interference-Causing Equipment Regulations.

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* The CE marking Declaration of Conformity contains important supplementary information and instructions for the user or installer.

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About This Manual

The *M Series User Manual* contains information about using the National Instruments M Series data acquisition (DAQ) devices with NI-DAQmx 8.7 and later. M Series devices feature up to 80 analog input (AI) channels, and up to four analog output (AO) channels, up to 48 lines of digital input/output (DIO), and two counters.

Conventions

The following conventions are used in this manual:

<>

Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

»

The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

This icon denotes a note, which alerts you to important information.

This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *Read Me First: Safety and Radio-Frequency Interference* for information about precautions to take.

bold

Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic

Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

`monospace`

Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories,

programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

Platform Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

Related Documentation

Each application software package and driver includes information about writing applications for taking measurements and controlling measurement devices. The following references to documents assume you have NI-DAQmx 8.7 or later, and where applicable, version 7.1 or later of the NI application software.

NI-DAQmx for Windows

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx for Windows software, how to install your NI-DAQmx-supported DAQ device, and how to confirm that your device is operating properly. Select **Start»All Programs»National Instruments»NI-DAQ»DAQ Getting Started Guide**.

The *NI-DAQ Readme* lists which devices are supported by this version of NI-DAQ. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQ Readme**.

The *NI-DAQmx Help* contains general information about measurement concepts, key NI-DAQmx concepts, and common applications that are applicable to all programming environments. Select **Start»All Programs» National Instruments»NI-DAQ»NI-DAQmx Help**.

NI-DAQmx for Linux

The *DAQ Getting Started Guide* describes how to install your NI-DAQmx-supported DAQ device and confirm that your device is operating properly.

The *NI-DAQ Readme for Linux* lists supported devices and includes software installation instructions, frequently asked questions, and known issues.

The *C Function Reference Help* describes functions and attributes.

The *NI-DAQmx for Linux Configuration Guide* provides configuration instructions, templates, and instructions for using test panels.

Note All NI-DAQmx documentation for Linux is installed at `/usr/local/natinst/nidaqmx/docs`.

Note USB-622*x*/625*x*/628*x* devices are *not* supported in NI-DAQmx for Linux.

NI-DAQmx Base (Linux/Mac OS X/LabVIEW PDA 8.*x*)

The *NI-DAQmx Base Getting Started Guide* describes how to install your NI-DAQmx Base software, your NI-DAQmx Base-supported DAQ device, and how to confirm that your device is operating properly. In Windows, select **Start»All Programs»National Instruments»NI-DAQmx Base»Documentation»Getting Started Guide**.

Getting Started with NI-DAQmx Base for Linux and Mac Users describes how to install your NI-DAQmx Base software, your NI-DAQmx Base-supported DAQ device, and how to confirm that your device is operating properly on your Mac/Linux machine.

The *NI-DAQmx Base Readme* lists which devices are supported by this version of NI-DAQmx Base. In Windows, select **Start»All Programs»National Instruments»NI-DAQmx Base»DAQmx Base Readme**.

The *NI-DAQmx Base VI Reference Help* contains VI reference and general information about measurement concepts. In LabVIEW, select **Help»NI-DAQmx Base VI Reference Help**.

The *NI-DAQmx Base C Reference Help* contains C reference and general information about measurement concepts. In Windows, select **Start»All Programs»National Instruments»NI-DAQmx Base»Documentation»C Function Reference Help**.

Note All NI-DAQmx Base documentation for Linux is installed at `/usr/local/natinst/nidaqmxbase/documentation`.

Note All NI-DAQmx Base documentation for Mac OS X is installed at `/Applications/National Instruments/NI-DAQmx Base/documentation`.

Note USB-622*x*/625*x*/628*x* devices are *not* supported in NI-DAQmx Base.

LabVIEW

If you are a new user, use the *Getting Started with LabVIEW* manual to familiarize yourself with the LabVIEW graphical programming environment and the basic LabVIEW features you use to build data acquisition and instrument control applications. Open the *Getting Started with LabVIEW* manual by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals** or by navigating to the `labview\manuals` directory and opening `LV_Getting_Started.pdf`.

Use the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help** in LabVIEW, to access information about LabVIEW programming concepts, step-by-step instructions for using LabVIEW, and reference information about LabVIEW VIs, functions, palettes, menus, and tools. Refer to the following locations on the **Contents** tab of the *LabVIEW Help* for information about NI-DAQmx:

- **Getting Started»Getting Started with DAQ**—Includes overview information and a tutorial to learn how to take an NI-DAQmx measurement in LabVIEW using the DAQ Assistant.
- **VI and Function Reference»Measurement I/O VIs and Functions**—Describes the LabVIEW NI-DAQmx VIs and properties.
- **Taking Measurements**—Contains the conceptual and how-to information you need to acquire and analyze measurement data in LabVIEW, including common measurements, measurement fundamentals, NI-DAQmx key concepts, and device considerations.

LabWindows/CVI

The **Data Acquisition** book of the *LabWindows/CVI Help* contains measurement concepts for NI-DAQmx. This book also contains *Taking an NI-DAQmx Measurement in LabWindows/CVI*, which includes step-by-step instructions about creating a measurement task using the DAQ Assistant. In LabWindows™/CVI™, select **Help»Contents**, then select **Using LabWindows/CVI»Data Acquisition**.

The **NI-DAQmx Library** book of the *LabWindows/CVI Help* contains API overviews and function reference for NI-DAQmx. Select **Library Reference»NI-DAQmx Library** in the *LabWindows/CVI Help*.

Measurement Studio

If you program your NI-DAQmx-supported device in Measurement Studio using Visual C++, Visual C#, or Visual Basic .NET, you can interactively create channels and tasks by launching the DAQ Assistant from MAX or from within Visual Studio .NET. You can generate the configuration code based on your task or channel in Measurement Studio. Refer to the *DAQ Assistant Help* for additional information about generating code. You also can create channels and tasks, and write your own applications in your ADE using the NI-DAQmx API.

For help with NI-DAQmx methods and properties, refer to the NI-DAQmx .NET Class Library or the NI-DAQmx Visual C++ Class Library included in the *NI Measurement Studio Help*. For general help with programming in Measurement Studio, refer to the *NI Measurement Studio Help*, which is fully integrated with the Microsoft Visual Studio .NET help. To view this help file in Visual Studio. NET, select **Measurement Studio» NI Measurement Studio Help**.

To create an application in Visual C++, Visual C#, or Visual Basic .NET, follow these general steps:

1. In Visual Studio .NET, select **File»New»Project** to launch the New Project dialog box.
2. Find the Measurement Studio folder for the language you want to create a program in.
3. Choose a project type. You add DAQ tasks as a part of this step.

ANSI C without NI Application Software

The *NI-DAQmx Help* contains API overviews and general information about measurement concepts. Select **Start»All Programs»National Instruments»NI-DAQ»NI-DAQmx Help**.

The *NI-DAQmx C Reference Help* describes the NI-DAQmx Library functions, which you can use with National Instruments data acquisition devices to develop instrumentation, acquisition, and control applications. Select **Start»All Programs»National Instruments»NI-DAQ» NI-DAQmx C Reference Help**.

.NET Languages without NI Application Software

With the Microsoft .NET Framework version 1.1 or later, you can use NI-DAQmx to create applications using Visual C# and Visual Basic .NET without Measurement Studio. You need Microsoft Visual Studio .NET 2003 or Microsoft Visual Studio 2005 for the API documentation to be installed.

The installed documentation contains the NI-DAQmx API overview, measurement tasks and concepts, and function reference. This help is fully integrated into the Visual Studio .NET documentation. To view the NI-DAQmx .NET documentation, go to **Start»Programs»National Instruments»NI-DAQ»NI-DAQmx .NET Reference Help**. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Reference** to view the function reference. Expand **NI Measurement Studio Help»NI Measurement Studio .NET Class Library»Using the Measurement Studio .NET Class Libraries** to view conceptual topics for using NI-DAQmx with Visual C# and Visual Basic .NET.

To get to the same help topics from within Visual Studio, go to **Help» Contents**. Select **Measurement Studio** from the **Filtered By** drop-down list and follow the previous instructions.

Device Documentation and Specifications

The *NI 622x Specifications* contains all specifications for the NI 6220, NI 6221, NI 6224, NI 6225, and NI 6229 M Series devices.

The *NI 625x Specifications* contains all specifications for the NI 6250, NI 6251, NI 6254, NI 6255, and NI 6259 M Series devices.

The *NI 628x Specifications* contains all specifications for the NI 6280, NI 6281, NI 6284, and NI 6289 M Series devices.

NI-DAQmx includes the Device Document Browser, which contains online documentation for supported DAQ and SCXI devices, such as documents describing device pinouts, features, and operation. You can find, view, and/or print the documents for each device using the Device Document Browser at any time by inserting the CD. After installing the Device Document Browser, device documents are accessible from **Start» All Programs»National Instruments»NI-DAQ»Browse Device Documentation**.

Training Courses

If you need more help getting started developing an application with NI products, NI offers training courses. To enroll in a course or obtain a detailed course outline, refer to `ni.com/training`.

Technical Support on the Web

For additional support, refer to `ni.com/support` or `zone.ni.com`.

Note You can download these documents at `ni.com/manuals`.

DAQ specifications and some DAQ manuals are available as PDFs. You must have Adobe Acrobat Reader with Search and Accessibility 5.0.5 or later installed to view the PDFs. Refer to the Adobe Systems Incorporated Web site at `www.adobe.com` to download Acrobat Reader. Refer to the National Instruments Product Manuals Library at `ni.com/manuals` for updated documentation resources.

1

Getting Started

M Series devices feature up to 80 analog input (AI) channels, up to four analog output (AO) channels, up to 48 lines of digital input/output (DIO), and two counters. If you have not already installed your device, refer to the *DAQ Getting Started Guide*. For specifications arranged by M Series device family, refer to the specifications document for your device on `ni.com/manuals`.

Before installing your DAQ device, you must install the software you plan to use with the device.

Installing NI-DAQmx

The *DAQ Getting Started Guide*, which you can download at `ni.com/manuals`, offers NI-DAQmx users step-by-step instructions for installing software and hardware, configuring channels and tasks, and getting started developing an application.

Installing Other Software

If you are using other software, refer to the installation instructions that accompany your software.

Installing the Hardware

The *DAQ Getting Started Guide* contains non-software-specific information about how to install PCI, PCI Express, PXI, PXI Express, and USB devices, as well as accessories and cables.

Device Self-Calibration

NI recommends that you self-calibrate your M Series device after installation and whenever the ambient temperature changes. Self-calibration should be performed after the device has warmed up for the recommended time period. Refer to the device specifications to find your device warm-up time. This function measures the onboard reference voltage of the device and adjusts the self-calibration constants to account for any errors caused by short-term fluctuations in the environment. Disconnect all external signals when you self-calibrate a device.

You can initiate self-calibration using Measurement & Automation Explorer (MAX), by completing the following steps.

1. Launch MAX.
2. Select **My System»Devices and Interfaces»NI-DAQmx Devices»*your device***.
3. Initiate self-calibration using one of the following methods:
   - Click **Self-Calibrate** in the upper right corner of MAX.
   - Right-click the name of the device in the MAX configuration tree and select **Self-Calibrate** from the drop-down menu.

Note You can also programmatically self-calibrate your device with NI-DAQmx, as described in *Device Calibration* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Device Pinouts

Refer to Appendix A, *Device-Specific Information*, for M Series device pinouts.

Device Specifications

Refer to the specifications for your device, the *NI 622x Specifications*, the *NI 625x Specifications*, or the *NI 628x Specifications*, available on the NI-DAQ Device Document Browser or `ni.com/manuals`, for more detailed information about M Series devices.

Device Accessories and Cables

NI offers a variety of accessories and cables to use with your DAQ device. Refer to Appendix A, *Device-Specific Information*, or `ni.com` for more information.

Applying the Signal Label to USB-62*xx* Screw Terminal Devices

(USB-622*x*/625*x*/628*x* Screw Terminal Devices) The supplied signal label can be adhered to the inside cover of the USB-62*xx* Screw Terminal device with supplied velcro strips as shown in Figure 1-1.

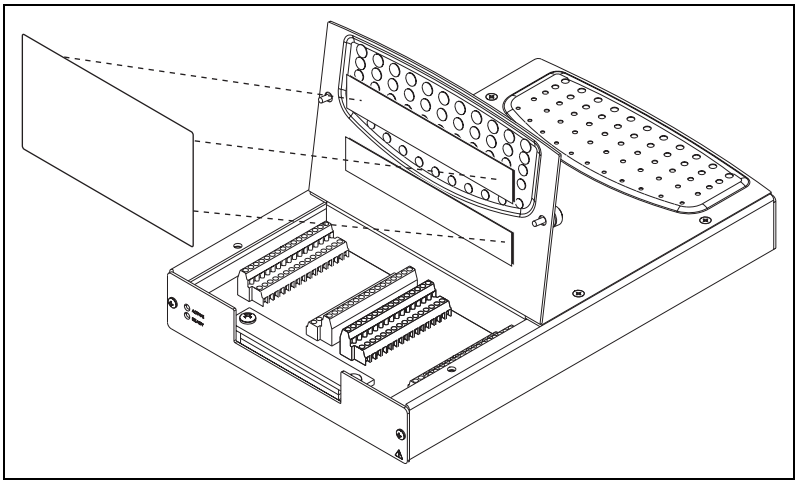


Figure 1-1. Applying the USB-62*xx* Screw Terminal Signal Label

USB Cable Strain Relief

(USB-622*x*/625*x*/628*x* Screw Terminal and USB-622*x*/625*x*/628*x* Mass Termination Devices) Use the supplied strain relief hardware to provide strain relief for your USB cable. Adhere the cable tie mount to the rear panel of the USB-62*xx* Screw Terminal or USB-62*xx* Mass Termination device, as shown in Figure 1-2. Thread a zip tie through the cable tie mount and tighten around the USB cable.

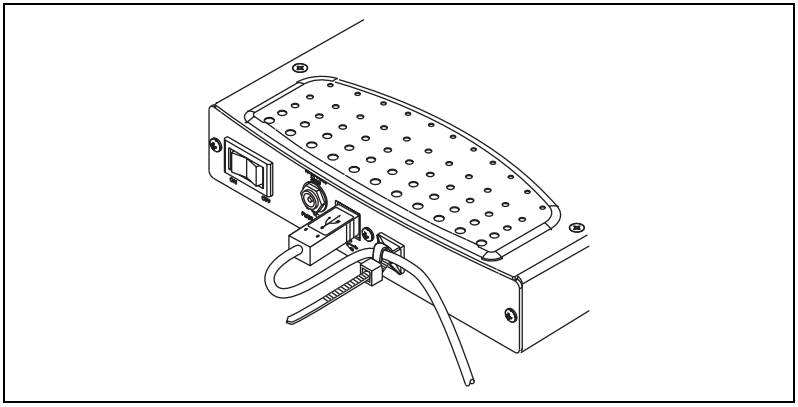


Figure 1-2. USB Cable Strain Relief on USB-62*xx* Screw Terminal and USB-62*xx* Mass Termination Devices

(USB-622*x*/625*x* BNC Devices) Thread a zip tie through two of the strain relief holes on the end cap to provide strain relief for your USB cable as shown in Figure 1-3. The strain relief holes can also be used as cable management for signal wires to/from the screw terminals and BNC connectors.

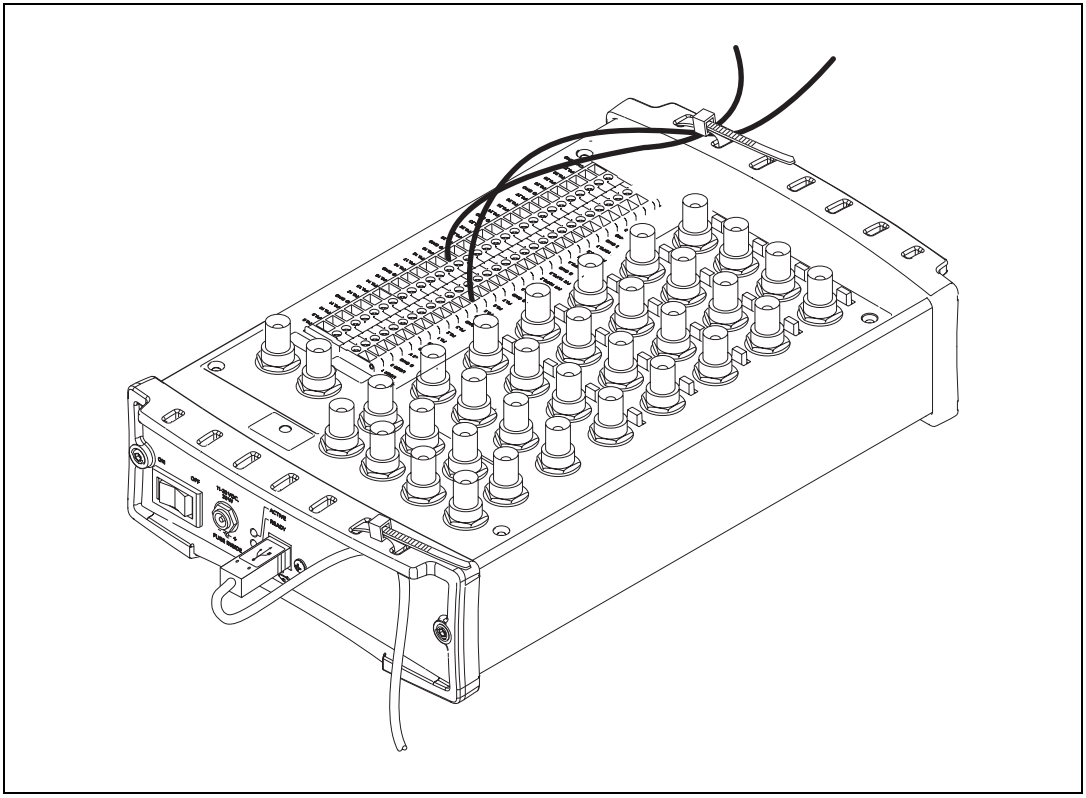


Figure 1-3. USB Cable Strain Relief on USB-62*xx* BNC Devices

USB Device Panel/Wall Mounting

(USB-622*x*/625*x*/628*x* Devices) The Externally Powered USB M Series Panel Mounting Kit (part number 780214-01, not included in your USB-62*xx* kit) is an accessory you can use to mount the USB-62*xx* family of products to a panel or wall.

2

DAQ System Overview

Figure 2-1 shows a typical DAQ system, which includes sensors, transducers, signal conditioning devices, cables that connect the various devices to the accessories, the M Series device, programming software, and PC. The following sections cover the components of a typical DAQ system.

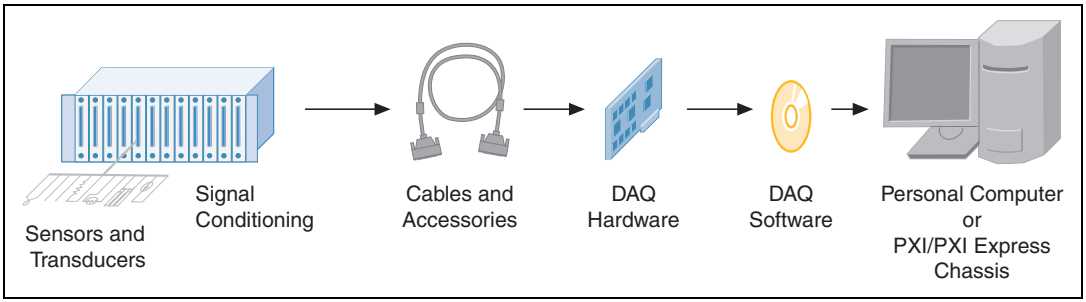


Figure 2-1. Components of a Typical DAQ System

DAQ Hardware

DAQ hardware digitizes signals, performs D/A conversions to generate analog output signals, and measures and controls digital I/O signals. Figure 2-2 features components common to all M Series devices.

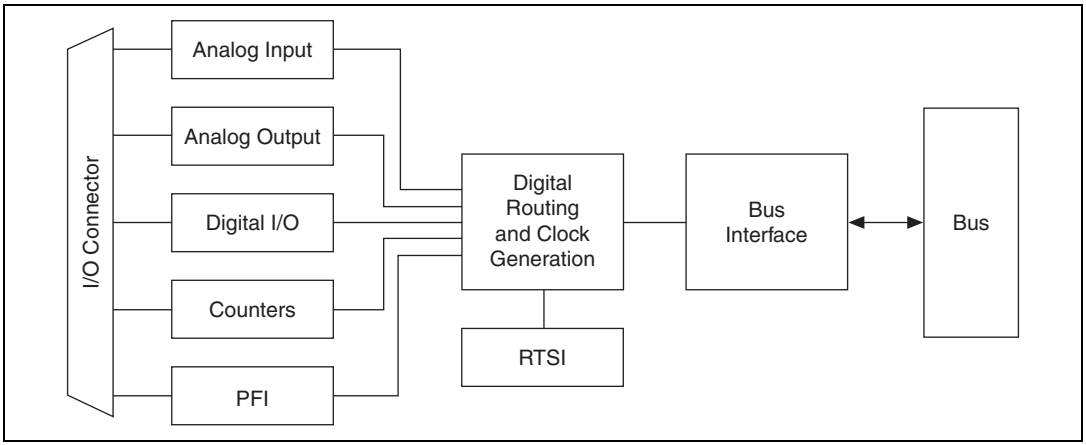


Figure 2-2. General M Series Block Diagram

DAQ-STC2 and DAQ-6202

The DAQ-STC2 and DAQ-6202 implement a high-performance digital engine for M Series data acquisition hardware. Some key features of this engine include the following:

- Flexible AI and AO sample and convert timing
- Many triggering modes
- Independent AI, AO, DI, and DO FIFOs
- Generation and routing of RTSI signals for multi-device synchronization
- Generation and routing of internal and external timing signals
- Two flexible 32-bit counter/timer modules with hardware gating
- Digital waveform acquisition and generation
- Static DIO signals
- True 5 V high current drive DO
- DI change detection
- PLL for clock synchronization

- Seamless interface to signal conditioning accessories
- PCI/PXI interface
- Independent scatter-gather DMA controllers for all acquisition and generation functions

Calibration Circuitry

The M Series analog inputs and outputs have calibration circuitry to correct gain and offset errors. You can calibrate the device to minimize AI and AO errors caused by time and temperature drift at run time. No external circuitry is necessary; an internal reference ensures high accuracy and stability over time and temperature changes.

Factory-calibration constants are permanently stored in an onboard EEPROM and cannot be modified. When you self-calibrate the device, software stores new constants in a user-modifiable section of the EEPROM. To return a device to its initial factory calibration settings, software can copy the factory-calibration constants to the user-modifiable section of the EEPROM. Refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information about using calibration constants.

For a detailed calibration procedure for M Series devices, refer to the *B/E/M/S Series Calibration Procedure for NI-DAQmx* by clicking **Manual Calibration Procedures** on `ni.com/calibration`.

Signal Conditioning

Many sensors and transducers require signal conditioning before a measurement system can effectively and accurately acquire the signal. The front-end signal conditioning system can include functions such as signal amplification, attenuation, filtering, electrical isolation, simultaneous sampling, and multiplexing. In addition, many transducers require excitation currents or voltages, bridge completion, linearization, or high amplification for proper and accurate operation. Therefore, most computer-based measurement systems include some form of signal conditioning in addition to plug-in data acquisition DAQ devices.

Sensors and Transducers

Sensors can generate electrical signals to measure physical phenomena, such as temperature, force, sound, or light. Some commonly used sensors are strain gauges, thermocouples, thermistors, angular encoders, linear encoders, and resistance temperature detectors (RTDs).

To measure signals from these various transducers, you must convert them into a form that a DAQ device can accept. For example, the output voltage of most thermocouples is very small and susceptible to noise. Therefore, you may need to amplify or filter the thermocouple output before digitizing it. The manipulation of signals to prepare them for digitizing is called *signal conditioning*.

For more information about sensors, refer to the following documents.

- For general information about sensors, visit `ni.com/sensors`.
- If you are using LabVIEW, refer to the *LabVIEW Help* by selecting **Help»Search the LabVIEW Help** in LabVIEW and then navigate to the **Taking Measurements** book on the **Contents** tab.
- If you are using other application software, refer to *Common Sensors* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Signal Conditioning Options

SCXI

SCXI is a front-end signal conditioning and switching system for various measurement devices, including M Series devices. An SCXI system consists of a rugged chassis that houses shielded signal conditioning modules that amplify, filter, isolate, and multiplex analog signals from thermocouples or other transducers. SCXI is designed for large measurement systems or systems requiring high-speed acquisition.

System features include the following.

- **Modular architecture**—Choose your measurement technology
- **Expandability**—Expand your system to 3,072 channels
- **Integration**—Combine analog input, analog output, digital I/O, and switching into a single, unified platform
- **High bandwidth**—Acquire signals at high rates
- **Connectivity**—Select from SCXI modules with thermocouple connectors or terminal blocks

Note SCXI is *not* supported on PCI-6221 (37-pin) or all variants of USB-622*x*/625*x*/628*x* devices.

SCC

SCC is a front-end signal conditioning system for M Series plug-in data acquisition devices. An SCC system consists of a shielded carrier that holds up to 20 single- or dual-channel SCC modules for conditioning thermocouples and other transducers. SCC is designed for small measurement systems where you need only a few channels of each signal type, or for portable applications. SCC systems also offer the most comprehensive and flexible signal connectivity options.

System features include the following.

- **Modular architecture**—Select your measurement technology on a per-channel basis
- **Small-channel systems**—Condition up to 16 analog input and eight digital I/O lines
- **Low-profile/portable**—Integrates well with other laptop computer measurement technologies
- **High bandwidth**—Acquire signals at rates up to 1.25 MHz
- **Connectivity**—Incorporates panelette technology to offer custom connectivity to thermocouple, BNC, LEMO™ (B Series), and MIL-Spec connectors

Note PCI Express users should consider the power limits on certain SCC modules without an external power supply. Refer to the specifications for your device, and the *Disk Drive Power Connector* section of Chapter 3, *Connector and LED Information*, for information about power limits and increasing the current the device can supply on the +5 V terminal.

Note SCC is *not* supported on the PCI-6221 (37-pin), USB-622*x*/625*x*/628*x* Screw Terminal, or USB-622*x*/625*x* BNC devices.

5B Series

5B is a front-end signal conditioning system for plug-in data acquisition devices. A 5B system consists of eight or 16 single-channel modules that plug into a backplane for conditioning thermocouples and other analog signals. National Instruments offers a complete line of 5B modules, carriers, backplanes, and accessories.

Note 5B is *not* supported on the PCI-6221 (37-pin), USB-622*x*/625*x*/628*x* Screw Terminal, or USB-622*x*/625*x* BNC devices.

Note For more information about SCXI, SCC, and 5B Series products, refer to `ni.com/signalconditioning`.

Cables and Accessories

NI offers a variety of products to use with M Series devices, including cables, connector blocks, and other accessories, as follows:

- Shielded cables and cable assemblies, and unshielded ribbon cables and cable assemblies
- Screw terminal connector blocks, shielded and unshielded
- RTSI bus cables
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals; with SCXI you can condition and acquire up to 3,072 channels
- Low-channel-count signal conditioning modules, devices, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold circuitry, and relays

For more specific information about these products, refer to `ni.com`.

Refer to the *Custom Cabling* section of this chapter, the *Field Wiring Considerations* section of Chapter 4, *Analog Input*, and Appendix A, *Device-Specific Information*, for information about how to select accessories for your M Series device.

Custom Cabling

NI offers cables and accessories for many applications. However, if you want to develop your own cable, adhere to the following guidelines for best results:

- For AI signals, use shielded, twisted-pair wires for each AI pair of differential inputs. Connect the shield for each signal pair to the ground reference at the source.
- Route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital sections of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

For more information about the connectors used for DAQ devices, refer to the KnowledgeBase document, *Specifications and Manufacturers for Board Mating Connectors*, by going to `ni.com/info` and entering the info code `rdspmb`.

Programming Devices in Software

National Instruments measurement devices are packaged with NI-DAQ driver software, an extensive library of functions and VIs you can call from your application software, such as LabVIEW or LabWindows/CVI, to program all the features of your NI measurement devices. Driver software has an application programming interface (API), which is a library of VIs, functions, classes, attributes, and properties for creating applications for your device.

NI-DAQ 7.3 and later includes two NI-DAQ drivers—Traditional NI-DAQ (Legacy) and NI-DAQmx. M Series devices use the NI-DAQmx driver. Each driver has its own API, hardware configuration, and software configuration. Refer to the *DAQ Getting Started Guide* for more information about the two drivers.

NI-DAQmx includes a collection of programming examples to help you get started developing an application. You can modify example code and save it in an application. You can use examples to develop a new application or add example code to an existing application.

To locate LabVIEW and LabWindows/CVI examples, open the National Instruments Example Finder. In LabVIEW and LabWindows/CVI, select **Help»Find Examples**.

Measurement Studio, Visual Basic, and ANSI C examples are located in the following directories:

- NI-DAQmx examples for Measurement Studio-supported languages are in the following directories:
  - `MeasurementStudio\VCNET\Examples\NIDaq`
  - `MeasurementStudio\DotNET\Examples\NIDaq`
- NI-DAQmx examples for ANSI C are in the `NI-DAQ\Examples\DAQmx ANSI C Dev` directory

For additional examples, refer to `zone.ni.com`.

3

Connector and LED Information

The *I/O Connector Signal Descriptions*, *M Series and E Series Pinout Comparison*, *+5 V Power Source*, *Disk Drive Power Connector*, and *RTSI Connector Pinout* sections contain information about M Series connectors. The *USB Device Fuse Replacement* and *LED Patterns* sections refer to M Series USB device fuses and LEDs. Refer to Appendix A, *Device-Specific Information*, for device I/O connector pinouts.

I/O Connector Signal Descriptions

Table 3-1 describes the signals found on the I/O connectors. Not all signals are available on all devices.

Table 3-1. I/O Connector Signals

Signal Name	Reference	Direction	Description
AI GND	—	—	**Analog Input Ground**—These terminals are the reference point for single-ended AI measurements in RSE mode and the bias current return point for DIFF measurements. All three ground references—AI GND, AO GND, and D GND—are connected on the device.
AI <0..79>	Varies	Input	**Analog Input Channels 0 to 79**—For single-ended measurements, each signal is an analog input voltage channel. In RSE mode, AI GND is the reference for these signals. In NRSE mode, the reference for each AI <0..15> signal is AI SENSE; the reference for each AI <16..63> and AI <64..79> signal is AI SENSE 2. For differential measurements, AI 0 and AI 8 are the positive and negative inputs of differential analog input channel 0. Similarly, the following signal pairs also form differential input channels: <AI 1, AI 9>, <AI 2, AI 10>, <AI 3, AI 11>, <AI 4, AI 12>, <AI 5, AI 13>, <AI 6, AI 14>, <AI 7, AI 15>, <AI 16, AI 24>, <AI 17, AI 25>, <AI 18, AI 26>, <AI 19, AI 27>, <AI 20, AI 28>, <AI 21, AI 29>, <AI 22, AI 30>, <AI 23, AI 31>, <AI 32, AI 40>, <AI 33, AI 41>, <AI 34, AI 42>, <AI 35, AI 43>, <AI 36, AI 44>, <AI 37, AI 45>, <AI 38, AI 46>, <AI 39, AI 47>, <AI 48, AI 56>, <AI 49, AI 57>, <AI 50, AI 58>, <AI 51, AI 59>, <AI 52, AI 60>, <AI 53, AI 61>, <AI 54, AI 62>, <AI 55, AI 63>, <AI 64, AI 72>, <AI 65, AI 73>, <AI 66, AI 74>, <AI 67, AI 75>, <AI 68, AI 76>, <AI 69, AI 77>, <AI 70, AI 78>, <AI 71, AI 79> Also refer to the *Connecting Ground-Referenced Signal Sources* section of Chapter 4, *Analog Input*.
AI SENSE, AI SENSE 2	—	Input	**Analog Input Sense**—In NRSE mode, the reference for each AI <0..15> signal is AI SENSE; the reference for each AI <16..63> and AI <64..79> signal is AI SENSE 2. Also refer to the *Connecting Ground-Referenced Signal Sources* section of Chapter 4, *Analog Input*

Table 3-1. I/O Connector Signals (Continued)

Signal Name	Reference	Direction	Description
AO <0..3>	AO GND	Output	**Analog Output Channels 0 to 3**—These terminals supply the voltage output of AO channels 0 to 3.
AO GND	—	—	**Analog Output Ground**—AO GND is the reference for AO <0..3>. All three ground references—AI GND, AO GND, and D GND—are connected on the device.
D GND	—	—	**Digital Ground**—D GND supplies the reference for P0.<0..31>, PFI <0..15>/P1/P2, and +5 V. All three ground references—AI GND, AO GND, and D GND—are connected on the device.
P0.<0..31>	D GND	Input or Output	**Port 0 Digital I/O Channels 0 to 31**—You can individually configure each signal as an input or output.
APFI <0..1>	AO GND/AI GND	Input	**Analog Programmable Function Interface Channels 0 to 1**—Each APFI signal can be used as AO external reference inputs for AO <0..3>, AO external offset input, or as an analog trigger input. APFI <0..1> are referenced to AI GND when they are used as analog trigger inputs. APFI <0..1> are referenced to AO GND when they are used as AO external offset or reference inputs. These functions are not available on all devices. Refer to the specifications for your device.
+5 V	D GND	Output	**+5 V Power Source**—These terminals provide a fused +5 V power source.
PFI <0..7>/P1.<0..7> PFI <8..15>/P2.<0..7>	D GND	Input or Output	**Programmable Function Interface or Digital I/O Channels 0 to 7 and Channels 8 to 15**—Each of these terminals can be individually configured as a PFI terminal or a digital I/O terminal. As an input, each PFI terminal can be used to supply an external source for AI, AO, DI, and DO timing signals or counter/timer inputs. As a PFI output, you can route many different internal AI, AO, DI, or DO timing signals to each PFI terminal. You also can route the counter/timer outputs to each PFI terminal. As a Port 1 or Port 2 digital I/O signal, you can individually configure each signal as an input or output.
USER <1..2>	—	—	**User-Defined Channels 1 and 2**—On USB-62*xx* BNC devices, the USER <1..2> BNC connectors allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER <1..2> BNC connectors are internally routed to the USER <1..2> screw terminals.

Table 3-1. I/O Connector Signals (Continued)

Signal Name	Reference	Direction	Description
CHS GND*	—	—	**Chassis Ground***—This terminal connects to the USB-62*xx* BNC device metal enclosure. You can connect your cable's shield wire to CHS GND for a ground connection.
NC	—	—	**No connect**—Do *not* connect signals to these terminals.
* USB-62*xx* Screw Terminal users can connect the shield of a shielded cable to the chassis ground lug for a ground connection. The chassis ground lug is not available on all device versions.			

M Series and E Series Pinout Comparison

The pinout of Connector 0 of 68-pin M Series devices is similar to the pinout of 68-pin E Series devices. On M Series devices, some terminals have enhanced functionality or other slight differences. Table 3-2 compares the two pinouts.

Table 3-2. M Series and E Series Device Pinout Comparison

Terminal	E Series Terminal*	M Series Terminal	Differences
1	FREQ OUT	PFI 14/P2.6	E Series devices drive each of these terminals with one particular internal timing signal. M Series devices can drive each terminal with the same signal as on E Series devices. On M Series devices, you also can route many other internal timing signals to each terminal. On M Series devices, you also can use these terminals as additional PFI inputs to drive internal timing signals. On M Series devices, you also can use these terminals as digital I/O signals. Also refer to Chapter 8, *PFI*.
2	CTR 0 OUT (GPCTR0_OUT)	PFI 12/P2.4	
40	CTR 1 OUT (GPCTR1_OUT)	PFI 13/P2.5	
45	EXT STROBE	PFI 10/P2.2	
46	AI HOLD COMP (SCANCLK)	PFI 11/P2.3	
3	PFI 9/CTR 0 GATE (GPCTR0_GATE)	PFI 9/P2.1	As a PFI input, the functionality of E Series and M Series devices is similar for these terminals. E Series devices can drive each of these terminals with one particular internal timing signal. M Series devices can drive each terminal with the same signal as on E Series devices. On M Series devices, you also can route many other internal timing signals to each terminal. On M Series devices, you also can use these terminals as digital I/O signals. Also refer to Chapter 8, *PFI*.
5	PFI 6/AO START TRIG (WFTRIG)	PFI 6/P1.6	
6	PFI 5/AO SAMP CLK (UPDATE)	PFI 5/P1.5	
10	PFI 1/AI REF TRIG (TRIG2)	PFI 1/P1.1	
37	PFI 8/CTR 0 SRC (GPCTR0_SOURCE)	PFI 8/P2.0	
38	PFI 7/AI SAMP CLK (STARTSCAN)	PFI 7/P1.7	
41	PFI 4/CTR 1 GATE (GPCTR1_GATE)	PFI 4/P1.4	
42	PFI 3/CTR 1 SRC (GPCTR1_SOURCE)	PFI 3/P1.3	
43	PFI 2/AI CONV CLK (CONVERT)	PFI 2/P1.2	

Table 3-2. M Series and E Series Device Pinout Comparison (Continued)

Terminal	E Series Terminal*	M Series Terminal	Differences
11	PFI 0/AI START TRIG (TRIG1)	PFI 0/P1.0	On E Series devices, as an input, this terminal can either be a PFI input or the analog trigger input. On M Series devices, as an input, this terminal can only be a PFI input. Analog triggers use the APFI <0..1> terminals. E Series devices can drive this terminal with the AI START TRIG signal. M Series devices, as an output, can drive this terminal with the AI START TRIG signal. You also can route many other internal timing signals to this terminal. On M Series devices, you also can use this terminal as the digital I/O signal, P1.0. Also refer to Chapter 8, *PFI*.
16	P0.6	P0.6	On both E Series and M Series devices, these terminals are digital I/O signals. You can individually configure each signal as an input or output. On E Series devices, P0.6 and P0.7 also can control the up/down signal of general-purpose Counters 0 and 1, respectively. On M Series devices, you have to use one of the PFI terminals to control the up/down signal of general-purpose Counters 0 and 1.
48	P0.7	P0.7	
20	AO EXT REF (EXTREF)	APFI 0	On E Series devices, this terminal is the external reference input for the AO circuitry. On M Series devices, this terminal can be used as the external reference input for the AO circuitry, the external offset for the AO circuitry, or the analog trigger input. These functions are not available on all devices. Refer to the specifications for your device. Note that this terminal is a no connect on some E Series and M Series devices.
39	D GND	PFI 15/P2.7	On E Series devices, this is one of the D GND terminals. On M Series devices, this is the PFI 15/P2.7 terminal.

* In NI-DAQmx, National Instruments has revised terminal names so they are easier to understand and more consistent among National Instruments hardware and software products. This column shows the NI-DAQmx terminal names (Traditional NI-DAQ (Legacy) terminal names are shown in parentheses).

Refer to Appendix D, *Upgrading from E Series to M Series*, for more information about the differences between these two device families.

+5 V Power Source

The +5 V terminals on the I/O connector supply +5 V referenced to D GND. Use these terminals to power external circuitry.

Newer revision M Series devices have a traditional fuse to protect the supply from overcurrent conditions. This fuse is not customer-replaceable; if the fuse permanently opens, return the device to NI for repair

Older revision M Series devices have a self-resetting fuse to protect the supply from overcurrent conditions. This fuse resets automatically within a few seconds after the overcurrent condition is removed. For more information about the self-resetting fuse and precautions to take to avoid improper connection of +5 V and ground terminals, refer to the KnowledgeBase document, *Self-Resetting Fuse Additional Information*, by going to `ni.com/info` and entering the info code `pptc`.

(USB-6281/6289 Devices) All USB-628*x* devices have a user-replaceable socketed fuse to protect the supply from overcurrent conditions. When an overcurrent condition occurs, check your cabling to the +5 V terminals and replace the fuse as described in the *USB Device Fuse Replacement* section.

Caution *Never* connect the +5 V power terminals to analog or digital ground or to any other voltage source on the M Series device or any other device. Doing so can damage the device and the computer. NI is *not* liable for damage resulting from such a connection.

The power rating on most devices is +4.75 to +5.25 VDC at 1 A.

Refer to the specifications document for your device to obtain the device power rating.

Note **(NI PCIe-625*x* Devices Only)** M Series PCI Express devices supply less than 1 A of +5 V power unless you use the disk drive power connector. Refer to the *Disk Drive Power Connector* section for more information.

Note The NI 6221 (37-pin) device does *not* have a +5 V terminal.

USB Chassis Ground

(USB-622*x*/625*x*/628*x* Devices Only) For EMC compliance, the chassis of the USB M Series device *must* be connected to earth ground through the chassis ground.

The wire should be AWG 16 or larger solid copper wire with a maximum length of 1.5 m (5 ft). Attach the wire to the earth ground of the facility's power system. For more information about earth ground connections, refer to the KnowledgeBase document, *Earth Grounding for Test and Measurement Devices*, by going to `ni.com/info` and entering the info code `earthground`.

You can attach a wire to the ground lug screw of any USB-62*xx* device, as shown in Figure 3-1.

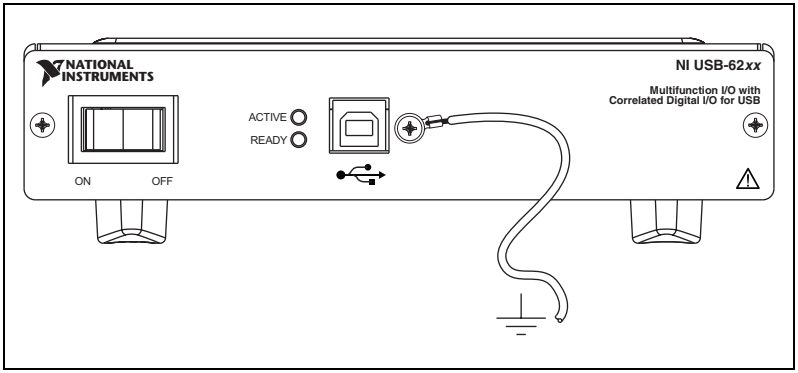


Figure 3-1. Grounding a USB-62*xx* Device through the Ground Lug Screw

(USB-6225/625*x*/628*x* Screw Terminal Devices Only) You can attach and solder a wire to the chassis ground lug of certain USB-62*xx* Screw Terminal devices, as shown in Figure 3-2. The wire should be as short as possible.

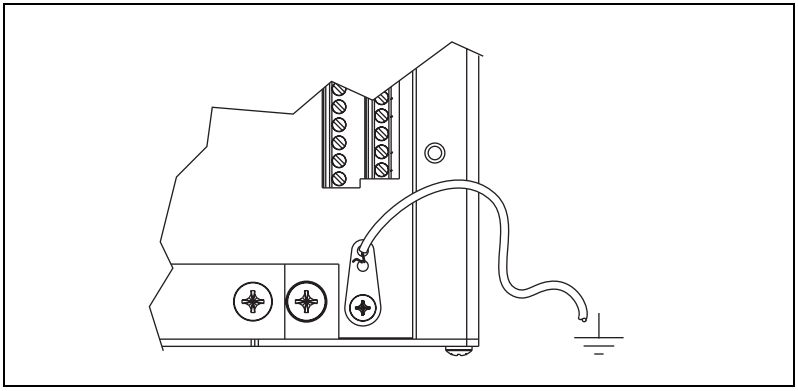


Figure 3-2. Grounding a USB-62*xx* Screw Terminal Device through the Chassis Ground Lug

(USB-62*xx* BNC Devices Only) You can attach a wire to a CHS GND screw terminal of any USB-62*xx* BNC device, as shown in Figure 3-3. Use as short a wire as possible. In addition, the wires in the shielded cable that extend beyond the shield should be as short as possible.

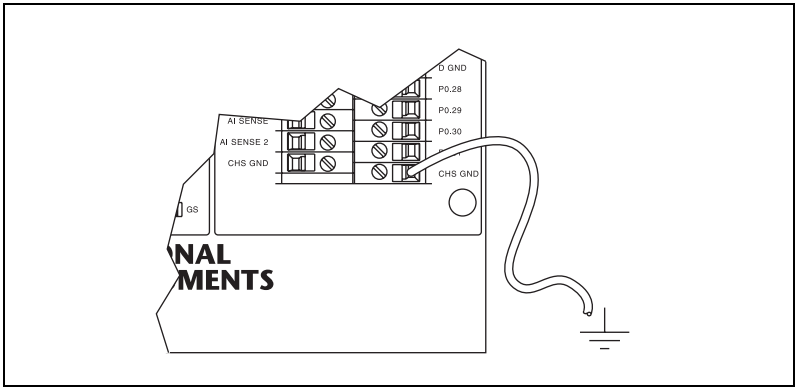


Figure 3-3. Grounding a USB-62*xx* BNC Device through the CHS GND Screw Terminal

Disk Drive Power Connector

(NI PCIe-625*x* Devices Only) The disk drive power connector is a four-pin hard drive connector on PCI Express devices that, when connected, increases the current the device can supply on the +5 V terminal.

When to Use the Disk Drive Power Connector

M Series PCI Express devices without the disk drive power connector installed perform identically to other M Series devices for most applications and with most accessories. For most applications, it is not necessary to install the disk drive power connector.

However, you should install the disk drive power connector in either of the following situations:

- You need more power than listed in the device specifications
- You are using an SCC accessory without an external power supply, such as the SC-2345

Refer to the specifications document for your device for more information about PCI Express power requirements and power limits.

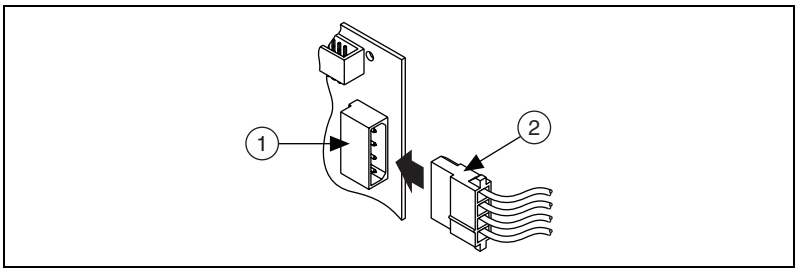
Disk Drive Power Connector Installation

Before installing the disk drive power connector, you must install and set up the M Series PCI Express device as described in the *DAQ Getting Started Guide*. Complete the following steps to install the disk drive power connector.

1. Power off and unplug the computer.
2. Remove the computer cover.

3. Attach the PC disk drive power connector to the disk drive power connector on the device, as shown in Figure 3-4.

Note The power available on the disk drive power connectors in a computer can vary. For example, consider using a disk drive power connector that is not in the same power chain as the hard drive.



1	Device Disk Drive Power Connector	2	PC Disk Drive Power Connector

Figure 3-4. Connecting to the Disk Drive Power Connector

4. Replace the computer cover, and plug in and power on the computer.
5. Self-calibrate the PCI Express DAQ device in MAX by following the instructions in the *Device Self-Calibration* section of Chapter 1, *Getting Started*.

Note Connecting or disconnecting the disk drive power connector can affect the analog performance of your device. To compensate for this, NI recommends that you self-calibrate after connecting or disconnecting the disk drive power connector.

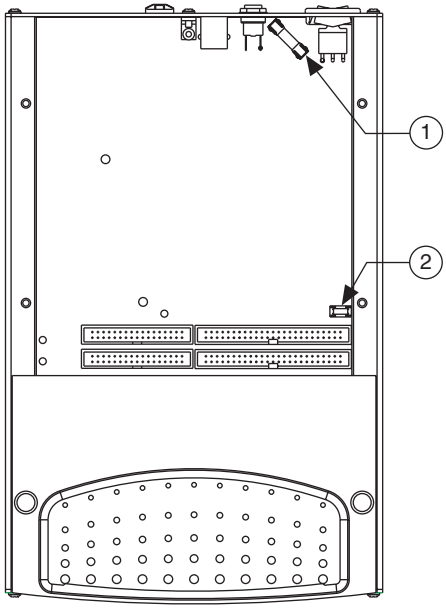
USB Device Fuse Replacement

M Series USB devices have a replaceable T 2A 250V (5 × 20 mm) fuse that protects the device from overcurrent through the power connector.

(USB-6281/6289 Devices) USB-628*x* devices also have a replaceable Littelfuse 0453002 (F 2A 250V) fuse that protects the device from overcurrent through the +5 V terminal(s).

(USB-622*x*/625*x*/628*x* Screw Terminal Devices) To replace a broken fuse in the USB-62*xx* Screw Terminal, complete the following steps.

1. Power down and unplug the device.
2. Loosen the four Phillips screws that attach the back lid to the enclosure, and remove the lid.
3. Replace the broken fuse while referring to Figure 3-5 for the fuse locations.



1	T 2A 250V (5 x 20 mm) Fuse	2	Littelfuse 0453002 Fuse on USB-628*x* Devices

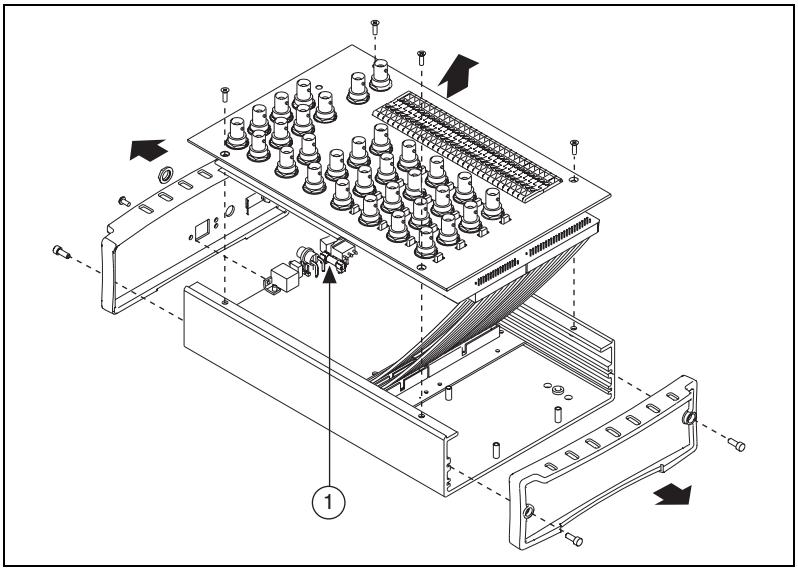
Figure 3-5. USB-62*xx* Screw Terminal Fuse Locations

4. Replace the lid and screws.

(USB-622*x*/625*x* BNC Devices) To replace a broken fuse in the USB-62*xx* BNC, complete the following steps.

1. Power down and unplug the device.

Note Take proper ESD precautions when handling the device.



1	T 2A 250V (5 x 20 mm) Fuse

Figure 3-6. USB-62*xx* BNC Fuse Location

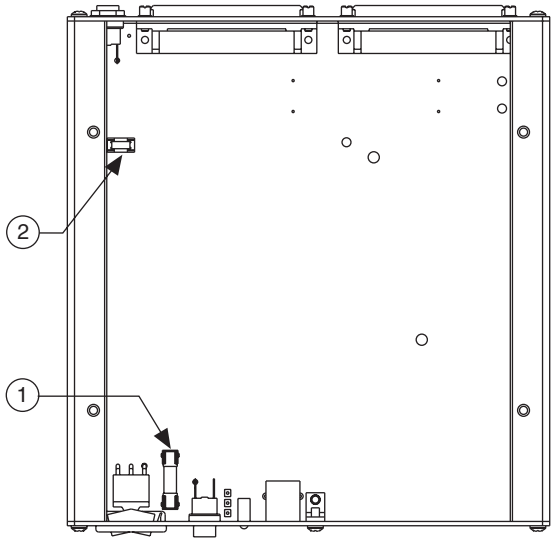
2. Remove both end pieces by unscrewing the four sockethead cap screws with a 7/64 in. hex wrench.

Note The end pieces are attached using self-threading screws. Repeated screwing and unscrewing of self-threading screws will produce a compromised connection.

3. With a Phillips #2 screwdriver, remove the Phillips 4-40 screw adjacent to the USB connector.
4. Remove the nut from the power connector.
5. Remove the four Phillips 4-40 screws that attach the top panel to the enclosure, and remove the panel and connector unit.
6. Replace the broken fuse while referring to Figure 3-6 for the fuse location.
7. Replace the top panel, screws, nut, and end pieces.

(USB-622*x*/625*x*/628*x* Mass Termination Devices) To replace a broken fuse in the USB-62*xx* Mass Termination, complete the following steps.

1. Power down and unplug the device.
2. Loosen the four Phillips screws that attach the lid to the enclosure and remove the lid.
3. Replace the broken fuse while referring to Figure 3-7 for the fuse locations.



1	T 2A 250V (5 x 20 mm) Fuse	2	Littelfuse 0453002 Fuse on USB-628*x* Devices

Figure 3-7. USB-62*xx* Mass Termination Fuse Locations

4. Replace the lid and screws.

RTSI Connector Pinout

Refer to the *RTSI Connector Pinout* section of Chapter 9, *Digital Routing and Clock Generation*, for information about the RTSI connector.

LED Patterns

(USB-62*xx* Devices Only) All variants of M Series USB devices have LEDs labeled ACTIVE and READY. The ACTIVE LED indicates activity over the bus. The READY LED indicates whether or not the device is configured. Table 3-3 shows the behavior of the LEDs.

Note USB-62*xx* BNC devices also have a POWER (+5 V) LED on the top panel. The POWER (+5 V) LED indicates device power.

Table 3-3. LED Patterns

POWER (+5 V) LED*	ACTIVE LED	READY LED	USB Device State
Off	Off	Off	The device is not powered.
On	Off	Off	The device is powered but not connected to the host computer.
On	Off	On	The device is configured, but there is no activity over the bus.
On	On	On	The device is configured and there is activity over the bus.
On	Blinking	On	

* The POWER (+5 V) LED is available on USB-62*xx* BNC devices only.

4

Analog Input

Figure 4-1 shows the analog input circuitry of M Series devices.

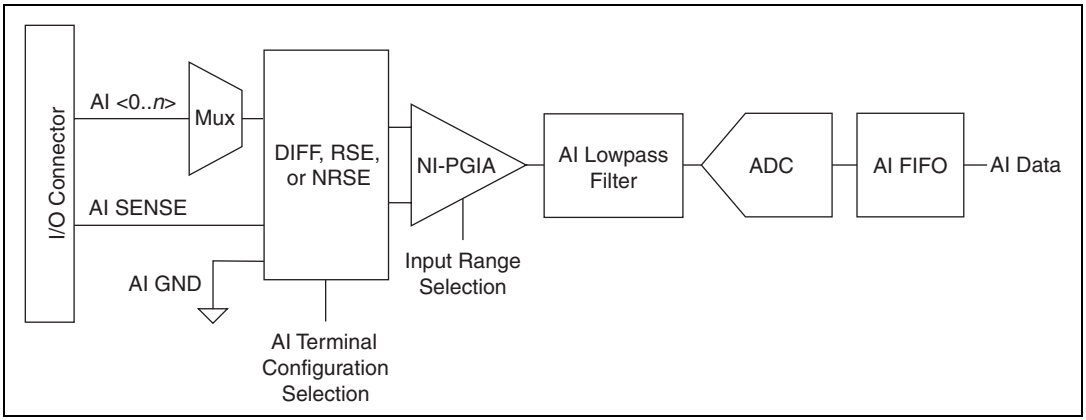


Figure 4-1. M Series Analog Input Circuitry

The main blocks featured in the M Series analog input circuitry are as follows:

- **I/O Connector**—You can connect analog input signals to the M Series device through the I/O connector. The proper way to connect analog input signals depends on the analog input ground-reference settings, described in the *Analog Input Ground-Reference Settings* section. Also refer to Appendix A, *Device-Specific Information*, for device I/O connector pinouts.
- **MUX**—Each M Series device has one analog-to-digital converter (ADC). The multiplexers (MUX) route one AI channel at a time to the ADC through the NI-PGIA.
- **Ground-Reference Settings**—The analog input ground-reference settings circuitry selects between differential, referenced single-ended, and non-referenced single-ended input modes. Each AI channel can use a different mode.
- **Instrumentation Amplifier (NI-PGIA)**—The NI programmable gain instrumentation amplifier (NI-PGIA) is a measurement and instrument class amplifier that minimizes settling times for all input ranges. The

NI-PGIA can amplify or attenuate an AI signal to ensure that you use the maximum resolution of the ADC.

M Series devices use the NI-PGIA to deliver high accuracy even when sampling multiple channels with small input ranges at fast rates. M Series devices can sample channels in any order at the maximum conversion rate, and you can individually program each channel in a sample with a different input range.

- **A/D Converter**—The analog-to-digital converter (ADC) digitizes the AI signal by converting the analog voltage into a digital number.
- **AI FIFO**—M Series devices can perform both single and multiple A/D conversions of a fixed or infinite number of samples. A large first-in-first-out (FIFO) buffer holds data during AI acquisitions to ensure that no data is lost. M Series devices can handle multiple A/D conversion operations with DMA, interrupts, or programmed I/O.

Analog Input Range

Input range refers to the set of input voltages that an analog input channel can digitize with the specified accuracy. The NI-PGIA amplifies or attenuates the AI signal depending on the input range. You can individually program the input range of each AI channel on your M Series device.

The input range affects the resolution of the M Series device for an AI channel. Resolution refers to the voltage of one ADC code. For example, a 16-bit ADC converts analog inputs into one of 65,536 (= 2^{16}) codes—that is, one of 65,536 possible digital values. These values are spread fairly evenly across the input range. So, for an input range of –10 V to 10 V, the voltage of each code of a 16-bit ADC is:

$$\frac{(10\text{ V} - (-10\text{ V}))}{2^{16}} = 305\ \mu\text{V}$$

M Series devices use a calibration method that requires some codes (typically about 5% of the codes) to lie outside of the specified range. This calibration method improves absolute accuracy, but it increases the nominal resolution of input ranges by about 5% over what the formula shown above would indicate.

Choose an input range that matches the expected input range of your signal. A large input range can accommodate a large signal variation, but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution, but may result in the input signal going out of range.

For more information about setting ranges, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Tables 4-1, 4-2, and 4-3 show the input ranges and resolutions supported by each M Series device family.

Table 4-1. Input Ranges for NI 622*x*

Input Range	Nominal Resolution Assuming 5% Over Range
–10 V to 10 V	320 µV
–5 V to 5 V	160 µV
–1 V to 1 V	32 µV
–200 mV to 200 mV	6.4 µV

Table 4-2. Input Ranges for NI 625*x*

Input Range	Nominal Resolution Assuming 5% Over Range
–10 V to 10 V	320 µV
–5 V to 5 V	160 µV
–2 V to 2 V	64 µV
–1 V to 1 V	32 µV
–500 mV to 500 mV	16 µV
–200 mV to 200 mV	6.4 µV
–100 mV to 100 mV	3.2 µV

Table 4-3. Input Ranges for NI 628*x*

Input Range	Nominal Resolution Assuming 5% Over Range
–10 V to 10 V	80.1 µV
–5 V to 5 V	40.1 µV
–2 V to 2 V	16.0 µV
–1 V to 1 V	8.01 µV
–500 mV to 500 mV	4.01 µV
–200 mV to 200 mV	1.60 µV
–100 mV to 100 mV	0.80 µV

Analog Input Lowpass Filter

A lowpass filter attenuates signals with frequencies above the cutoff frequency while passing, with minimal attenuation, signals below the cutoff frequency. The cutoff frequency is defined as the frequency at which the output amplitude has decreased by 3 dB. Lowpass filters attenuate noise and reduce aliasing of signals beyond the Nyquist frequency. For example, if the signal of interest does not have frequency components beyond 40 kHz, then using a filter with a cutoff frequency at 40 kHz will attenuate noise beyond the cutoff that is not of interest. The cutoff frequency of the lowpass filter is also called the small signal bandwidth. The specifications document for your DAQ device lists the small signal bandwidth.

On some devices, the filter cutoff is fixed. On other devices, this filter is programmable and can be enabled for a lower frequency. For example, the NI 628*x* devices have a programmable filter with a cutoff frequency of 40 kHz that can be enabled. If the programmable filter is not enabled, the cutoff frequency is fixed at 750 kHz. If the cutoff is programmable, choose the lower cutoff to reduce measurement noise. However, a filter with a lower cutoff frequency increases the settling time of your device, as shown in the specifications, which reduces its maximum conversion rate. Therefore, you may have to reduce the rate of your AI Convert and AI Sample Clocks. If that reduced sample rate is too slow for your application, select the higher cutoff frequency.

Add additional filters to AI signals using external accessories, as described in the *Cables and Accessories* section of Chapter 2, *DAQ System Overview*.

Analog Input Ground-Reference Settings

M Series devices support the analog input ground-reference settings shown in Table 4-4.

Table 4-4. Analog Input Ground-Reference Settings

AI Ground-Reference Settings	Description
DIFF	In differential (DIFF) mode, the M Series device measures the difference in voltage between two AI signals.
RSE	In referenced single-ended (RSE) mode, the M Series device measures the voltage of an AI signal relative to AI GND.
NRSE	In non-referenced single-ended (NRSE) mode, the M Series device measures the voltage of an AI signal relative to one of the AI SENSE or AI SENSE 2 inputs.

The *AI ground-reference* setting determines how you should connect your AI signals to the M Series device. Refer to the *Connecting Analog Input Signals* section for more information.

Ground-reference settings are programmed on a per-channel basis. For example, you might configure the device to scan 12 channels—four differentially-configured channels and eight single-ended channels.

M Series devices implement the different analog input ground-reference settings by routing different signals to the NI-PGIA. The NI-PGIA is a differential amplifier. That is, the NI-PGIA amplifies (or attenuates) the difference in voltage between its two inputs. The NI-PGIA drives the ADC with this amplified voltage. The amount of amplification (the gain), is determined by the analog input range, as shown in Figure 4-2.

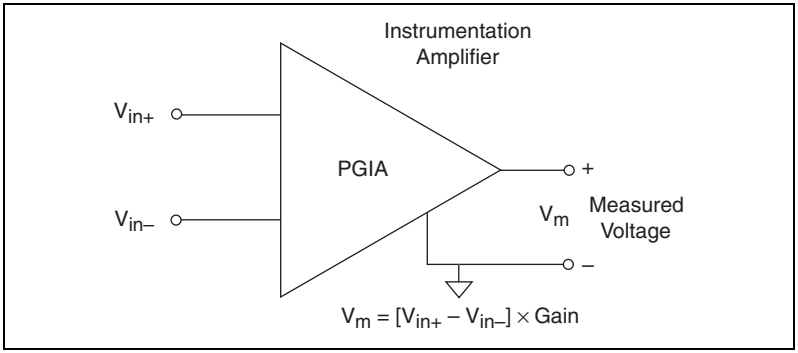


Figure 4-2. NI-PGIA

Table 4-5 shows how signals are routed to the NI-PGIA.

Table 4-5. Signals Routed to the NI-PGIA

AI Ground-Reference Settings	Signals Routed to the Positive Input of the NI-PGIA (V_{in+})	Signals Routed to the Negative Input of the NI-PGIA (V_{in-})
RSE	AI <0..79>	AI GND
NRSE	AI <0..15>	AI SENSE
	AI <16..79>	AI SENSE 2
DIFF	AI <0..7>	AI <8..15>
	AI <16..23>	AI <24..31>
	AI <32..39>, AI <48..55>, AI <64..71>	AI <40..47>, AI <56..63>, AI <72..79>

Notice that some M Series devices do not support the AI <16..79> signals.

For differential measurements, AI 0 and AI 8 are the positive and negative inputs of differential analog input channel 0. For a complete list of signal pairs that form differential input channels, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Caution The maximum input voltages rating of AI signals with respect to ground (and for differential signals with respect to each other) are listed in the specifications document for your device. Exceeding the maximum input voltage of AI signals distorts the measurement results. Exceeding the maximum input voltage rating also can damage the device and the computer. NI is *not* liable for any damage resulting from such signal connections.

AI ground-reference setting is sometimes referred to as *AI terminal configuration*.

Configuring AI Ground-Reference Settings in Software

You can program channels on an M Series device to acquire with different ground references.

To enable multimode scanning in LabVIEW, use `NI-DAQmx Create Virtual Channel.vi` of the NI-DAQmx API. You must use a new VI for each channel or group of channels configured in a different input mode. In Figure 4-3, channel 0 is configured in differential mode, and channel 1 is configured in RSE mode.

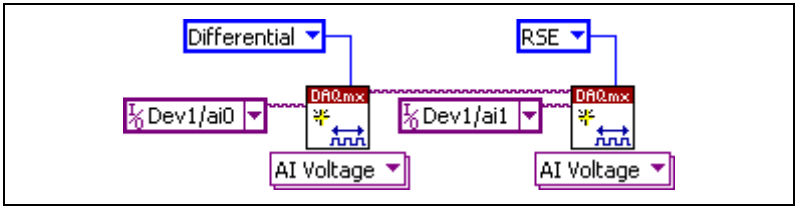


Figure 4-3. Enabling Multimode Scanning in LabVIEW

To configure the input mode of your voltage measurement using the DAQ Assistant, use the **Terminal Configuration** drop-down list. Refer to the *DAQ Assistant Help* for more information about the DAQ Assistant.

To configure the input mode of your voltage measurement using the NI-DAQmx C API, set the **terminalConfig** property. Refer to the *NI-DAQmx C Reference Help* for more information.

Multichannel Scanning Considerations

M Series devices can scan multiple channels at high rates and digitize the signals accurately. However, you should consider several issues when designing your measurement system to ensure the high accuracy of your measurements.

In multichannel scanning applications, accuracy is affected by settling time. When your M Series device switches from one AI channel to another AI channel, the device configures the NI-PGIA with the input range of the new channel. The NI-PGIA then amplifies the input signal with the gain for the new input range. Settling time refers to the time it takes the NI-PGIA to

amplify the input signal to the desired accuracy before it is sampled by the ADC. The specifications document for your DAQ device lists its settling time.

M Series devices are designed to have fast settling times. However, several factors can increase the settling time which decreases the accuracy of your measurements. To ensure fast settling times, you should do the following (in order of importance):

- Use Low Impedance Sources
- Use Short High-Quality Cabling
- Carefully Choose the Channel Scanning Order
- Avoid Scanning Faster Than Necessary

Use Low Impedance Sources

To ensure fast settling times, your signal sources should have an impedance of <1 kΩ. Large source impedances increase the settling time of the NI-PGIA, and so decrease the accuracy at fast scanning rates.

Settling times increase when scanning high-impedance signals due to a phenomenon called charge injection. Multiplexers contain switches, usually made of switched capacitors. When one of the channels, for example channel 0, is selected in a multiplexer, those capacitors accumulate charge. When the next channel, for example channel 1, is selected, the accumulated charge leaks backward through channel 1. If the output impedance of the source connected to channel 1 is high enough, the resulting reading of channel 1 can be partially affected by the voltage on channel 0. This effect is referred to as ghosting.

If your source impedance is high, you can decrease the scan rate to allow the NI-PGIA more time to settle. Another option is to use a voltage follower circuit external to your DAQ device to decrease the impedance seen by the DAQ device. Refer to the KnowledgeBase document, *How Do I Create a Buffer to Decrease the Source Impedance of My Analog Input Signal?*, by going to `ni.com/info` and entering the info code `rdbbis`.

Use Short High-Quality Cabling

Using short high-quality cables can minimize several effects that degrade accuracy including crosstalk, transmission line effects, and noise. The capacitance of the cable also can increase the settling time.

National Instruments recommends using individually shielded, twisted-pair wires that are 2 m or less to connect AI signals to the device. Refer to the *Connecting Analog Input Signals* section for more information.

Carefully Choose the Channel Scanning Order

Avoid Switching from a Large to a Small Input Range

Switching from a channel with a large input range to a channel with a small input range can greatly increase the settling time.

Suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1. The input range for channel 0 is –10 V to 10 V and the input range of channel 1 is –200 mV to 200 mV.

When the multiplexer switches from channel 0 to channel 1, the input to the NI-PGIA switches from 4 V to 1 mV. The approximately 4 V step from 4 V to 1 mV is 1,000% of the new full-scale range. For a 16-bit device to settle within 0.0015% (15 ppm or 1 LSB) of the ±200 mV full-scale range on channel 1, the input circuitry must settle to within 0.000031% (0.31 ppm or 1/50 LSB) of the ±10 V range. Some devices can take many microseconds for the circuitry to settle this much.

To avoid this effect, you should arrange your channel scanning order so that transitions from large to small input ranges are infrequent.

In general, you do not need this extra settling time when the NI-PGIA is switching from a small input range to a larger input range.

Insert Grounded Channel between Signal Channels

Another technique to improve settling time is to connect an input channel to ground. Then insert this channel in the scan list between two of your signal channels. The input range of the grounded channel should match the input range of the signal after the grounded channel in the scan list.

Consider again the example above where a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1. Suppose the input range for channel 0 is –10 V to 10 V and the input range of channel 1 is –200 mV to 200 mV.

You can connect channel 2 to AI GND (or you can use the internal ground; refer to *Internal Channels* in the *NI-DAQmx Help*). Set the input range of channel 2 to –200 mV to 200 mV to match channel 1. Then scan channels in the order: 0, 2, 1.

Inserting a grounded channel between signal channels improves settling time because the NI-PGIA adjusts to the new input range setting faster when the input is grounded.

Minimize Voltage Step between Adjacent Channels

When scanning between channels that have the same input range, the settling time increases with the voltage step between the channels. If you know the expected input range of your signals, you can group signals with similar expected ranges together in your scan list.

For example, suppose all channels in a system use a –5 to 5 V input range. The signals on channels 0, 2, and 4 vary between 4.3 V and 5 V. The signals on channels 1, 3, and 5 vary between –4 V and 0 V. Scanning channels in the order 0, 2, 4, 1, 3, 5 produces more accurate results than scanning channels in the order 0, 1, 2, 3, 4, 5.

Avoid Scanning Faster Than Necessary

Designing your system to scan at slower speeds gives the NI-PGIA more time to settle to a more accurate level. Here are two examples to consider.

Example 1

Averaging many AI samples can increase the accuracy of the reading by decreasing noise effects. In general, the more points you average, the more accurate the final result. However, you may choose to decrease the number of points you average and slow down the scanning rate.

Suppose you want to sample 10 channels over a period of 20 ms and average the results. You could acquire 500 points from each channel at a scan rate of 250 kS/s. Another method would be to acquire 1,000 points from each channel at a scan rate of 500 kS/s. Both methods take the same amount of time. Doubling the number of samples averaged (from 500 to 1,000) decreases the effect of noise by a factor of 1.4 (the square root of 2). However, doubling the number of samples (in this example) decreases the time the NI-PGIA has to settle from 4 µs to 2 µs. In some cases, the slower scan rate system returns more accurate results.

Example 2

If the time relationship between channels is not critical, you can sample from the same channel multiple times and scan less frequently. For example, suppose an application requires averaging 100 points from channel 0 and averaging 100 points from channel 1. You could alternate reading between channels—that is, read one point from channel 0, then one point from channel 1, and so on. You also could read all 100 points from channel 0 then read 100 points from channel 1. The second method switches between channels much less often and is affected much less by settling time.

Analog Input Data Acquisition Methods

When performing analog input measurements, you either can perform software-timed or hardware-timed acquisitions. Hardware-timed acquisitions can be buffered or non-buffered.

Software-Timed Acquisitions

With a software-timed acquisition, software controls the rate of the acquisition. Software sends a separate command to the hardware to initiate each ADC conversion. In NI-DAQmx, software-timed acquisitions are referred to as having on-demand timing. Software-timed acquisitions are also referred to as immediate or static acquisitions and are typically used for reading a single sample of data.

Hardware-Timed Acquisitions

With hardware-timed acquisitions, a digital hardware signal (ai/SampleClock) controls the rate of the acquisition. This signal can be generated internally on your device or provided externally.

Hardware-timed acquisitions have several advantages over software-timed acquisitions.

- The time between samples can be much shorter.
- The timing between samples is deterministic.
- Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or non-buffered. A buffer is a temporary storage in computer memory for to-be-generated samples.

Buffered

In a buffered acquisition, data is moved from the DAQ device's onboard FIFO memory to a PC buffer using DMA or interrupts before it is transferred to application memory. Buffered acquisitions typically allow for much faster transfer rates than non-buffered acquisitions because data is moved in large blocks, rather than one point at a time.

One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous.

Finite sample mode acquisition refers to the acquisition of a specific, predetermined number of data samples. Once the specified number of samples has been read in, the acquisition stops. If you use a reference trigger, you must use finite sample mode.

Continuous acquisition refers to the acquisition of an unspecified number of samples. Instead of acquiring a set number of data samples and stopping, a continuous acquisition continues until you stop the operation. Continuous acquisition is also referred to as *double-buffered* or *circular-buffered acquisition*.

If data cannot be transferred across the bus fast enough, the FIFO becomes full. New acquisitions will overwrite data in the FIFO before it can be transferred to host memory. The device generates an error in this case. With continuous operations, if the user program does not read data out of the PC buffer fast enough to keep up with the data transfer, the buffer could reach an overflow condition, causing an error to be generated.

Non-Buffered

In non-buffered acquisitions, data is read directly from the FIFO on the device. Typically, hardware-timed, non-buffered operations are used to read single samples with known time increments between them.

Analog Input Triggering

Analog input supports three different triggering actions:

- Start trigger
- Reference trigger
- Pause trigger

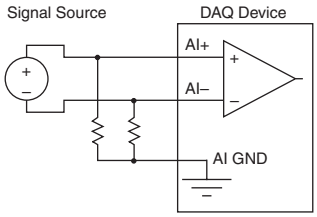
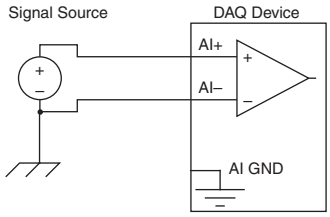
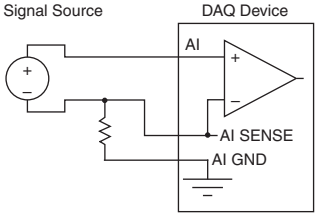
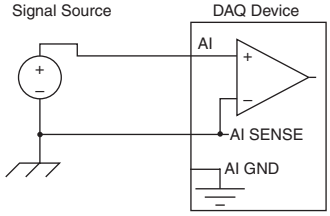
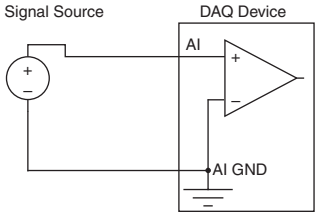
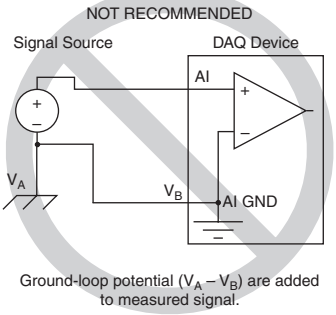
Refer to the *AI Start Trigger Signal*, *AI Reference Trigger Signal*, and *AI Pause Trigger Signal* sections for information about these triggers.

An analog or digital trigger can initiate these actions. All M Series devices support digital triggering, but some do not support analog triggering. To find your device triggering options, refer to the specifications document for your device.

Connecting Analog Input Signals

Table 4-6 summarizes the recommended input configuration for both types of signal sources.

Table 4-6. Analog Input Configuration

AI Ground-Reference Setting*	Floating Signal Sources (Not Connected to Building Ground)	Ground-Referenced Signal Sources†
	Examples: • Ungrounded thermocouples • Signal conditioning with isolated outputs • Battery devices	Example: • Plug-in instruments with non-isolated outputs
Differential		
Non-Referenced Single-Ended (NRSE)		
Referenced Single-Ended (RSE)		

* Refer to the *Analog Input Ground-Reference Settings* section for descriptions of the RSE, NRSE, and DIFF modes and software considerations.

† Refer to the *Connecting Ground-Referenced Signal Sources* section for more information.

Connecting Floating Signal Sources

What Are Floating Signal Sources?

A *floating signal source* is not connected to the building ground system, but has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolators, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source.

When to Use Differential Connections with Floating Signal Sources

Use DIFF input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the device are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.
- Two analog input channels, AI+ and AI–, are available for the signal.

DIFF signal connections reduce noise pickup and increase common-mode noise rejection. DIFF signal connections also allow input signals to float within the common-mode limits of the NI-PGIA.

Refer to the *Using Differential Connections for Floating Signal Sources* section for more information about differential connections.

When to Use Non-Referenced Single-Ended (NRSE) Connections with Floating Signal Sources

Only use NRSE input connections if the input signal meets the following conditions.

- The input signal is high-level (greater than 1 V).
- The leads connecting the signal to the device are less than 3 m (10 ft).

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

In the single-ended modes, more electrostatic and magnetic noise couples into the signal connections than in DIFF configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

With this type of connection, the NI-PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground.

Refer to the *Using Non-Referenced Single-Ended (NRSE) Connections for Floating Signal Sources* section for more information about NRSE connections.

When to Use Referenced Single-Ended (RSE) Connections with Floating Signal Sources

Only use RSE input connections if the input signal meets the following conditions.

- The input signal can share a common reference point, AI GND, with other signals that use RSE.
- The input signal is high-level (greater than 1 V).
- The leads connecting the signal to the device are less than 3 m (10 ft).

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

In the single-ended modes, more electrostatic and magnetic noise couples into the signal connections than in DIFF configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

With this type of connection, the NI-PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground.

Refer to the *Using Referenced Single-Ended (RSE) Connections for Floating Signal Sources* section for more information about RSE connections.

Using Differential Connections for Floating Signal Sources

It is important to connect the negative lead of a floating source to AI GND (either directly or through a bias resistor). Otherwise, the source may float out of the maximum working voltage range of the NI-PGIA and the DAQ device returns erroneous data.

The easiest way to reference the source to AI GND is to connect the positive side of the signal to AI+ and connect the negative side of the signal to AI GND as well as to AI– without using resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

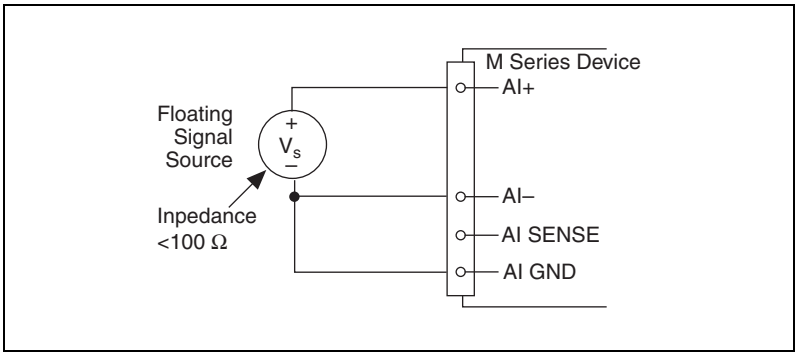


Figure 4-4. Differential Connections for Floating Signal Sources without Bias Resistors

However, for larger source impedances, this connection leaves the DIFF signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. This noise appears as a DIFF-mode signal instead of a common-mode signal, and thus appears in your data. In this case, instead of directly connecting the negative line to AI GND, connect the negative line to AI GND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. This configuration does not load down the source (other than the very high input impedance of the NI-PGIA).

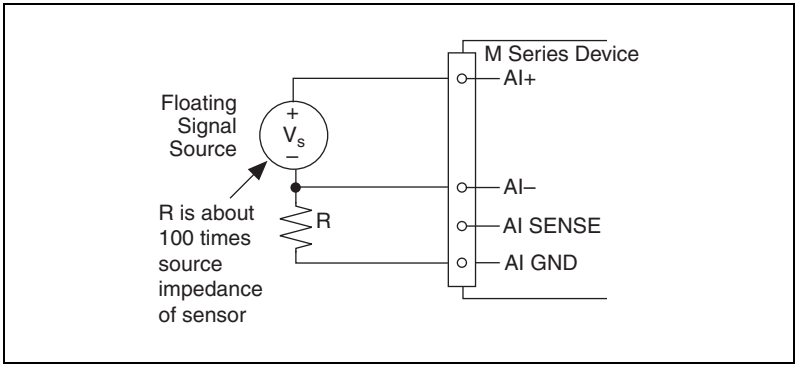


Figure 4-5. Differential Connections for Floating Signal Sources with Single Bias Resistor

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AI GND, as shown in Figure 4-6. This fully balanced configuration offers slightly better noise rejection, but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

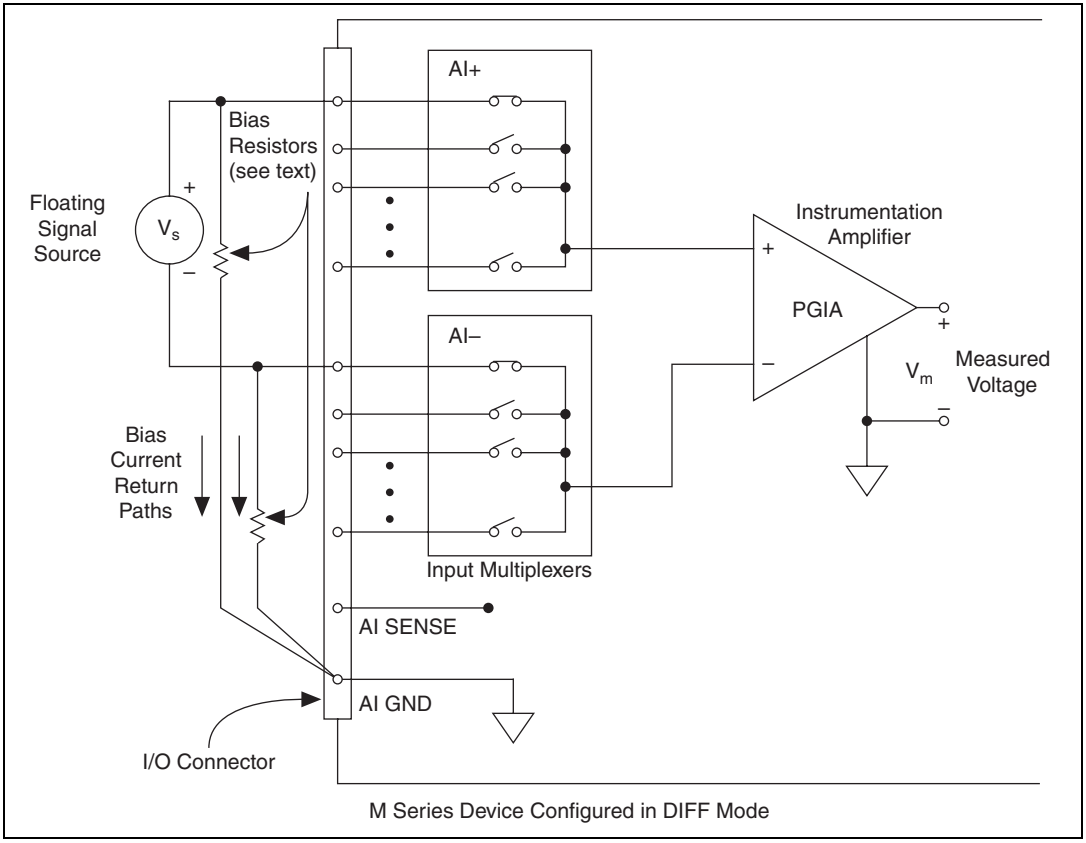


Figure 4-6. Differential Connections for Floating Signal Sources with Balanced Bias Resistors

Both inputs of the NI-PGIA require a DC path to ground in order for the NI-PGIA to work. If the source is AC coupled (capacitively coupled), the NI-PGIA needs a resistor between the positive input and AI GND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, connect the negative input directly to AI GND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs; be aware that there is some gain error from loading down the source, as shown in Figure 4-7.

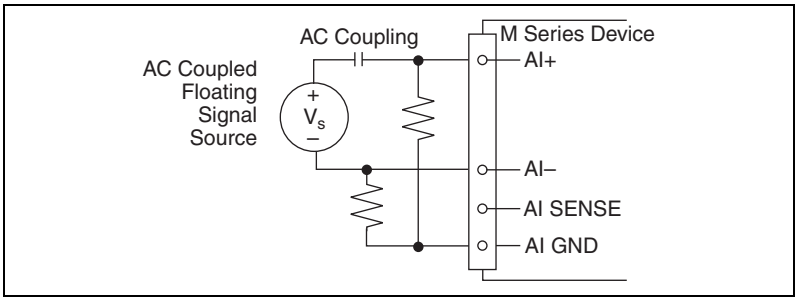


Figure 4-7. Differential Connections for AC Coupled Floating Sources with Balanced Bias Resistors

Using Non-Referenced Single-Ended (NRSE) Connections for Floating Signal Sources

It is important to connect the negative lead of a floating signals source to AI GND (either directly or through a resistor). Otherwise the source may float out of the valid input range of the NI-PGIA and the DAQ device returns erroneous data.

Figure 4-8 shows a floating source connected to the DAQ device in NRSE mode.

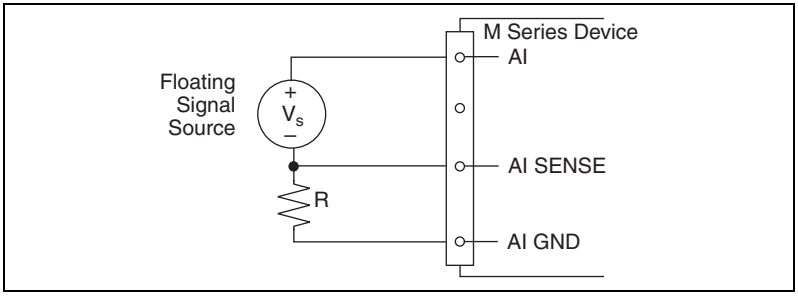


Figure 4-8. NRSE Connections for Floating Signal Sources

All of the bias resistor configurations discussed in the *Using Differential Connections for Floating Signal Sources* section apply to the NRSE bias resistors as well. Replace AI– with AI SENSE in Figures 4-4, 4-5, 4-6, and 4-7 for configurations with zero to two bias resistors. The noise rejection of NRSE mode is better than RSE mode because the AI SENSE connection is made remotely near the source. However, the noise rejection of NRSE mode is worse than DIFF mode because the AI SENSE connection is shared with all channels rather than being cabled in a twisted pair with the AI+ signal.

Using the DAQ Assistant, you can configure the channels for RSE or NRSE input modes. Refer to the *Configuring AI Ground-Reference Settings in Software* section for more information about the DAQ Assistant.

Using Referenced Single-Ended (RSE) Connections for Floating Signal Sources

Figure 4-9 shows how to connect a floating signal source to the M Series device configured for RSE mode.

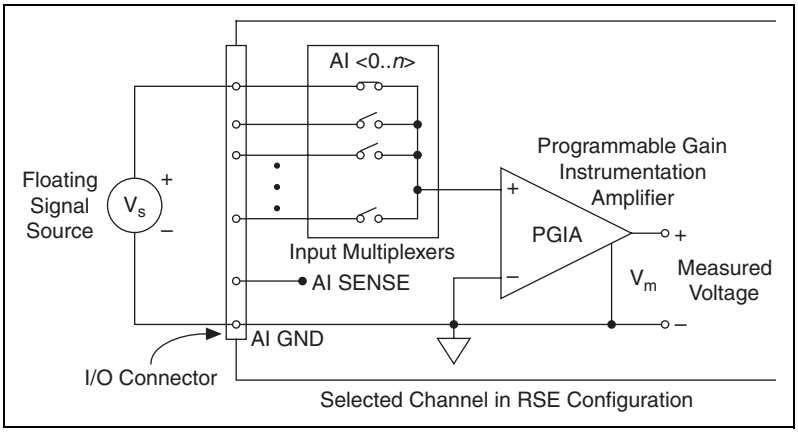


Figure 4-9. RSE Connections for Floating Signal Sources

Using the DAQ Assistant, you can configure the channels for RSE or NRSE input modes. Refer to the *Configuring AI Ground-Reference Settings in Software* section for more information about the DAQ Assistant.

Connecting Ground-Referenced Signal Sources

What Are Ground-Referenced Signal Sources?

A *ground-referenced signal source* is a signal source connected to the building system ground. It is already connected to a common ground point with respect to the device, assuming that the computer is plugged into the same power system as the source. Non-isolated outputs of instruments and devices that plug into the building power system fall into this category.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV, but the difference can be much higher if power distribution circuits are improperly connected. If a grounded signal source is incorrectly measured, this difference can appear as measurement error. Follow the connection instructions for grounded signal sources to eliminate this ground potential difference from the measured signal.

When to Use Differential Connections with Ground-Referenced Signal Sources

Use DIFF input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the device are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.
- Two analog input channels, AI+ and AI–, are available.

DIFF signal connections reduce noise pickup and increase common-mode noise rejection. DIFF signal connections also allow input signals to float within the common-mode limits of the NI-PGIA.

Refer to the *Using Differential Connections for Ground-Referenced Signal Sources* section for more information about differential connections.

When to Use Non-Referenced Single-Ended (NRSE) Connections with Ground-Referenced Signal Sources

Only use non-referenced single-ended input connections if the input signal meets the following conditions.

- The input signal is high-level (greater than 1 V).
- The leads connecting the signal to the device are less than 3 m (10 ft).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

In the single-ended modes, more electrostatic and magnetic noise couples into the signal connections than in DIFF configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

With this type of connection, the NI-PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground.

Refer to the *Using Non-Referenced Single-Ended (NRSE) Connections for Ground-Referenced Signal Sources* section for more information about NRSE connections.

When to Use Referenced Single-Ended (RSE) Connections with Ground-Referenced Signal Sources

Do *not* use RSE connections with ground-referenced signal sources. Use NRSE or DIFF connections instead.

As shown in the bottom-rightmost cell of Table 4-6, there can be a potential difference between AI GND and the ground of the sensor. In RSE mode, this ground loop causes measurement errors.

Using Differential Connections for Ground-Referenced Signal Sources

Figure 4-10 shows how to connect a ground-referenced signal source to the M Series device configured in DIFF mode.

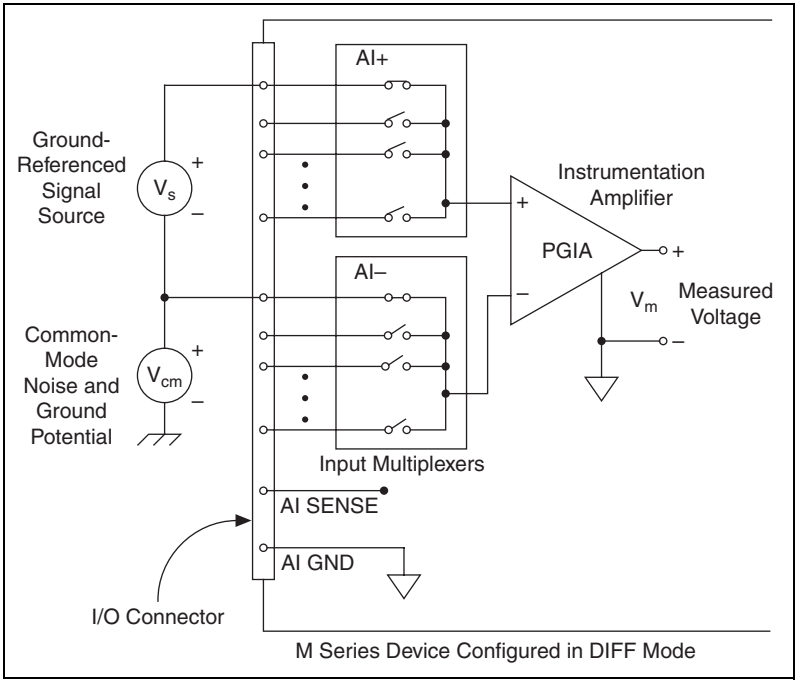


Figure 4-10. Differential Connections for Ground-Referenced Signal Sources

With this type of connection, the NI-PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground, shown as V_{cm} in the figure.

AI+ and AI– must both remain within ±11 V of AI GND.

Using Non-Referenced Single-Ended (NRSE) Connections for Ground-Referenced Signal Sources

Figure 4-11 shows how to connect ground-reference signal sources in NRSE mode.

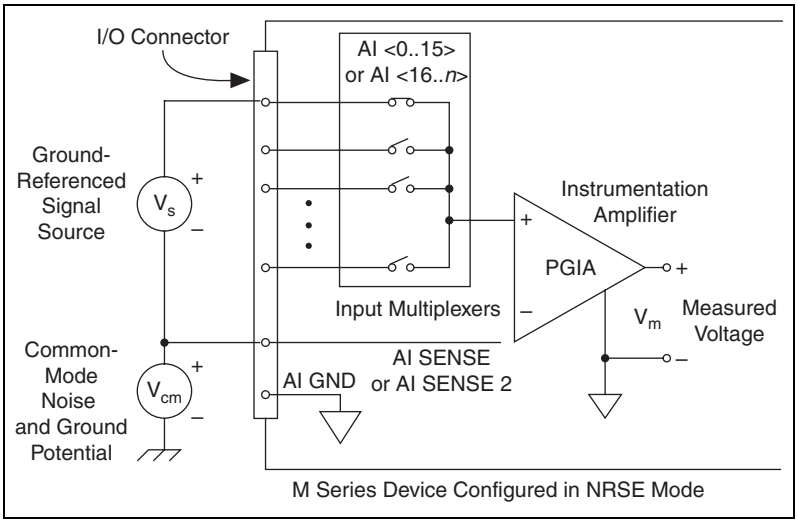


Figure 4-11. Single-Ended Connections for Ground-Referenced Signal Sources (NRSE Configuration)

AI+ and AI– must both remain within ±11 V of AI GND.

To measure a single-ended, ground-referenced signal source, you must use the NRSE ground-reference setting. Connect the signal to one of AI <0..15> and connect the signal local ground reference to AI SENSE. You also can connect the signal to one of AI <16..79> and connect the signal local ground reference to AI SENSE 2. AI SENSE (or AI SENSE 2) is internally connected to the negative input of the NI-PGIA. Therefore, the ground point of the signal connects to the negative input of the NI-PGIA.

Any potential difference between the device ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the NI-PGIA, and this difference is rejected by the amplifier. If the

input circuitry of a device were referenced to ground, as it is in the RSE ground-reference setting, this difference in ground potentials would appear as an error in the measured voltage.

Using the DAQ Assistant, you can configure the channels for RSE or NRSE input modes. Refer to the *Configuring AI Ground-Reference Settings in Software* section for more information about the DAQ Assistant.

Field Wiring Considerations

Environmental noise can seriously affect the measurement accuracy of the device if you do not take proper care when running signal wires between signal sources and the device. The following recommendations apply mainly to AI signal routing to the device, although they also apply to signal routing in general.

Minimize noise pickup and maximize measurement accuracy by taking the following precautions.

- Use DIFF AI connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect AI signals to the device. With this type of wire, the signals attached to the positive and negative input channels are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.

Refer to the NI Developer Zone document, *Field Wiring and Noise Considerations for Analog Signals*, for more information. To access this document, go to `ni.com/info` and enter the info code `rdfwn3`.

Analog Input Timing Signals

In order to provide all of the timing functionality described throughout this section, M Series devices have a flexible timing engine. Figure 4-12 summarizes all of the timing options provided by the analog input timing engine. Also refer to the *Clock Routing* section of Chapter 9, *Digital Routing and Clock Generation*.

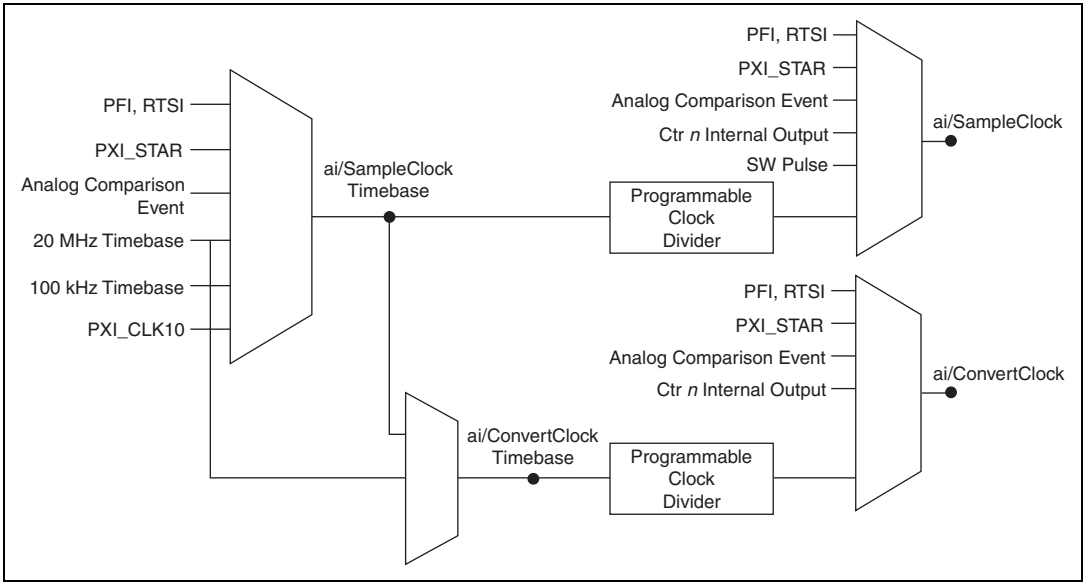


Figure 4-12. Analog Input Timing Options

M Series devices use ai/SampleClock and ai/ConvertClock to perform interval sampling. As Figure 4-13 shows, ai/SampleClock controls the sample period, which is determined by the following equation:

1/Sample Period = Sample Rate

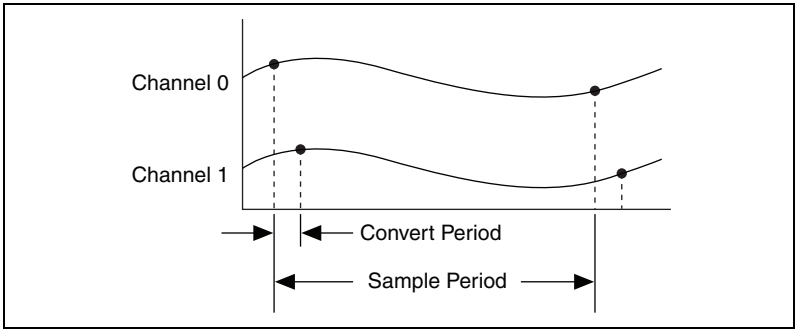


Figure 4-13. Interval Sampling

ai/ConvertClock controls the Convert Period, which is determined by the following equation:

1/Convert Period = Convert Rate

Typically, this rate is the sampling rate for the task multiplied by the number of channels in the task.

Note The sampling rate is the fastest you can acquire data on the device and still achieve accurate results. For example, if an M Series device has a sampling rate of 250 kS/s, this sampling rate is aggregate—one channel at 250 kS/s or two channels at 125 kS/s per channel illustrates the relationship.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered DAQ sequence is shown in Figure 4-14. The sample counter is loaded with the specified number of posttrigger samples, in this example, five. The value decrements with each pulse on ai/SampleClock, until the value reaches zero and all desired samples have been acquired.

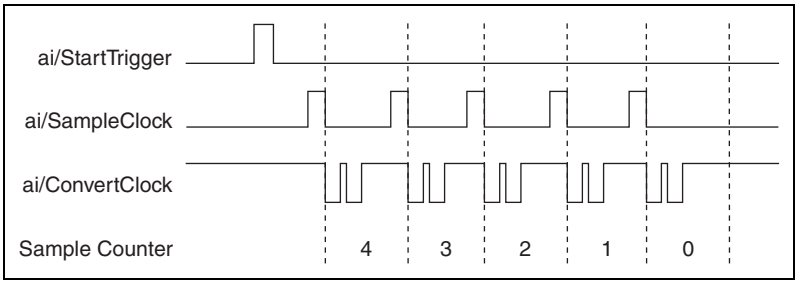


Figure 4-14. Posttriggered Data Acquisition Example

Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest, in addition to data acquired after the trigger. Figure 4-15 shows a typical pretriggered DAQ sequence. ai/StartTrigger can be either a hardware or software signal. If ai/StartTrigger is set up to be a software start trigger, an output pulse appears on the ai/StartTrigger line when the acquisition begins. When the ai/StartTrigger pulse occurs, the sample counter is loaded with the number of pretriggered samples, in this example, four. The value decrements with each pulse on ai/SampleClock, until the value reaches zero. The sample counter is then loaded with the number of posttriggered samples, in this example, three.

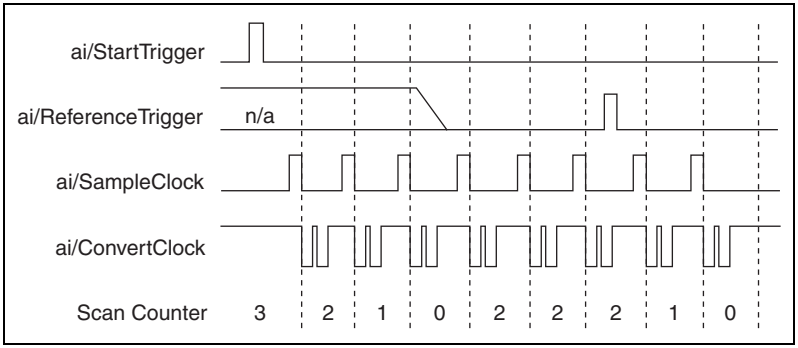


Figure 4-15. Pretriggered Data Acquisition Example

If an ai/ReferenceTrigger pulse occurs before the specified number of pretrigger samples are acquired, the trigger pulse is ignored. Otherwise, when the ai/ReferenceTrigger pulse occurs, the sample counter value decrements until the specified number of posttrigger samples have been acquired.

M Series devices feature the following analog input timing signals.

- AI Sample Clock Signal
- AI Sample Clock Timebase Signal
- AI Convert Clock Signal
- AI Convert Clock Timebase Signal
- AI Hold Complete Event Signal
- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Pause Trigger Signal

AI Sample Clock Signal

Use the AI Sample Clock (ai/SampleClock) signal to initiate a set of measurements. Your M Series device samples the AI signals of every channel in the task once for every ai/SampleClock. A measurement acquisition consists of one or more samples.

You can specify an internal or external source for ai/SampleClock. You also can specify whether the measurement sample begins on the rising edge or falling edge of ai/SampleClock.

Using an Internal Source

One of the following internal signals can drive ai/SampleClock.

- Counter *n* Internal Output
- AI Sample Clock Timebase (divided down)
- A pulse initiated by host software

A programmable internal counter divides down the sample clock timebase.

Several other internal signals can be routed to ai/SampleClock through RTSI. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Using an External Source

Use one of the following external signals as the source of ai/SampleClock:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR
- Analog Comparison Event (an analog trigger)

Routing AI Sample Clock Signal to an Output Terminal

You can route ai/SampleClock out to any PFI <0..15> or RTSI <0..7> terminal. This pulse is always active high.

You can specify the output to have one of two behaviors. With the pulse behavior, your DAQ device briefly pulses the PFI terminal once for every occurrence of ai/SampleClock.

With level behavior, your DAQ device drives the PFI terminal high during the entire sample.

All PFI terminals are configured as inputs by default.

Other Timing Requirements

Your DAQ device only acquires data during an acquisition. The device ignores ai/SampleClock when a measurement acquisition is not in progress. During a measurement acquisition, you can cause your DAQ device to ignore ai/SampleClock using the ai/PauseTrigger signal.

A counter on your device internally generates ai/SampleClock unless you select some external source. ai/StartTrigger starts this counter and either software or hardware can stop it once a finite acquisition completes. When using an internally generated ai/SampleClock, you also can specify a configurable delay from ai/StartTrigger to the first ai/SampleClock pulse. By default, this delay is set to two ticks of the ai/SampleClockTimebase signal. When using an externally generated ai/SampleClock, you must ensure the clock signal is consistent with respect to the timing requirements of ai/ConvertClock. Failure to do so may result in ai/SampleClock pulses that are masked off and acquisitions with erratic sampling intervals. Refer to AI Convert Clock Signal for more information about the timing requirements between ai/ConvertClock and ai/SampleClock.

Figure 4-16 shows the relationship of ai/SampleClock to ai/StartTrigger.

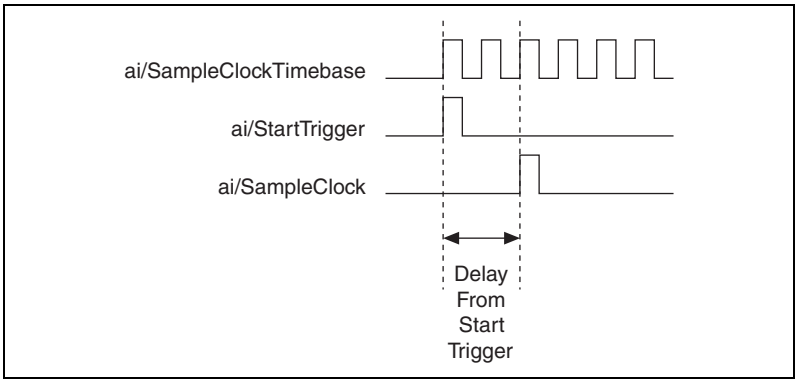


Figure 4-16. ai/SampleClock and ai/StartTrigger

AI Sample Clock Timebase Signal

You can route any of the following signals to be the AI Sample Clock Timebase (ai/SampleClockTimebase) signal:

- 20 MHz Timebase
- 100 kHz Timebase
- PXI_CLK10
- RTSI <0..7>
- PFI <0..15>
- PXI_STAR
- Analog Comparison Event (an analog trigger)

ai/SampleClockTimebase is not available as an output on the I/O connector. ai/SampleClockTimebase is divided down to provide one of the possible sources for ai/SampleClock. You can configure the polarity selection for ai/SampleClockTimebase as either rising or falling edge.

AI Convert Clock Signal

Use the AI Convert Clock (ai/ConvertClock) signal to initiate a single A/D conversion on a single channel. A sample (controlled by the AI Sample Clock) consists of one or more conversions.

You can specify either an internal or external signal as the source of ai/ConvertClock. You also can specify whether the measurement sample begins on the rising edge or falling edge of ai/ConvertClock.

With NI-DAQmx 7.4 and later, the driver chooses the fastest conversion rate possible based on the speed of the A/D converter and adds 10 µs of padding between each channel to allow for adequate settling time. This scheme enables the channels to approximate simultaneous sampling and still allow for adequate settling time. If the AI Sample Clock rate is too fast to allow for this 10 µs of padding, NI-DAQmx chooses the conversion rate so that the AI Convert Clock pulses are evenly spaced throughout the sample.

With NI-DAQmx 7.3, the driver chooses a conversion rate so the AI Convert Clock pulses are evenly spaced throughout the sample. This allows for the maximum settling time between conversions. To approximate simultaneous sampling, manually increase the conversion rate.

To explicitly specify the conversion rate, use **AI Convert Clock Rate DAQmx Timing** property node or function.

Caution Setting the conversion rate higher than the maximum rate specified for your device will result in errors.

Using an Internal Source

One of the following internal signals can drive ai/ConvertClock:

- AI Convert Clock Timebase (divided down)
- Counter *n* Internal Output

A programmable internal counter divides down the AI Convert Clock Timebase to generate ai/ConvertClock. The counter is started by ai/SampleClock and continues to count down to zero, produces an ai/ConvertClock, reloads itself, and repeats the process until the sample is finished. It then reloads itself in preparation for the next ai/SampleClock pulse.

Using an External Source

Use one of the following external signals as the source of ai/ConvertClock:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR
- Analog Comparison Event (an analog trigger)

Routing AI Convert Clock Signal to an Output Terminal

You can route ai/ConvertClock (as an active low signal) out to any PFI <0..15> or RTSI <0..7> terminal.

All PFI terminals are configured as inputs by default.

Using a Delay from Sample Clock to Convert Clock

When using an internally generated ai/ConvertClock, you also can specify a configurable delay from ai/SampleClock to the first ai/ConvertClock pulse within the sample. By default, this delay is three ticks of ai/ConvertClockTimebase.

Figure 4-17 shows the relationship of ai/SampleClock to ai/ConvertClock.

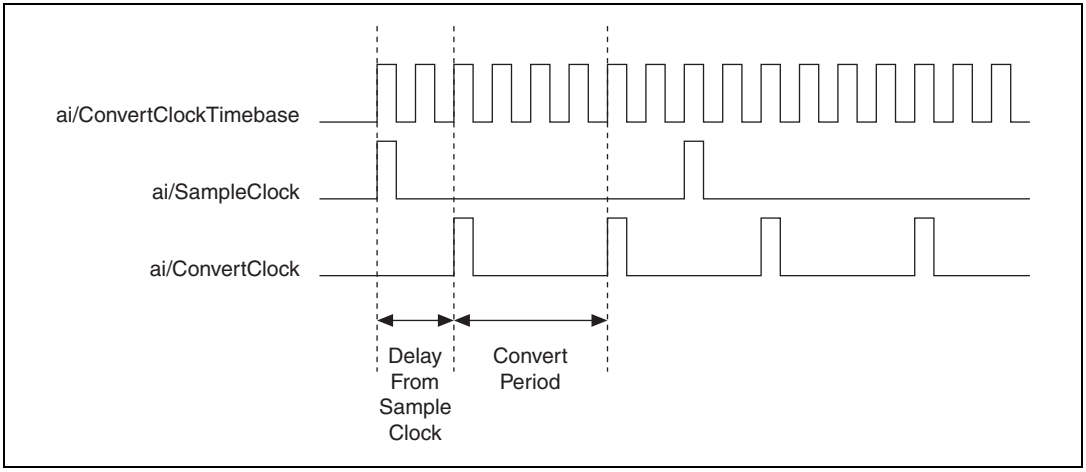


Figure 4-17. ai/SampleClock and ai/ConvertClock

Other Timing Requirements

The sample and conversion level timing of M Series devices work such that clock signals are gated off unless the proper timing requirements are met. For example, the device ignores both ai/SampleClock and ai/ConvertClock until it receives a valid ai/StartTrigger signal. Once the device recognizes an ai/SampleClock pulse, it ignores subsequent ai/SampleClock pulses until it receives the correct number of ai/ConvertClock pulses.

Similarly, the device ignores all ai/ConvertClock pulses until it recognizes an ai/SampleClock pulse. Once the device receives the correct number of ai/ConvertClock pulses, it ignores subsequent ai/ConvertClock pulses until it receives another ai/SampleClock. Figures 4-18, 4-19, 4-20, and 4-21 show timing sequences for a four-channel acquisition (using AI channels 0, 1, 2, and 3) and demonstrate proper and improper sequencing of ai/SampleClock and ai/ConvertClock.

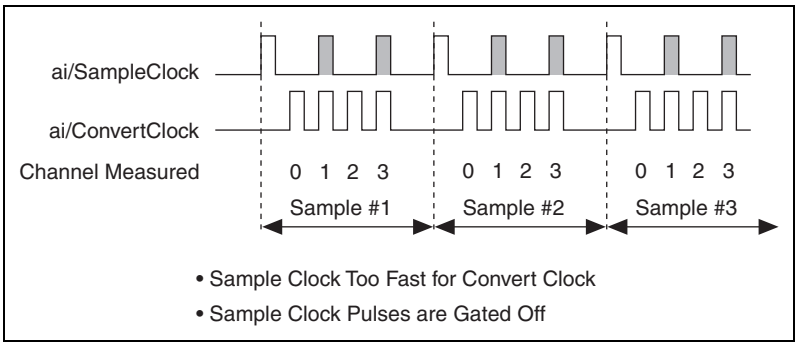


Figure 4-18. ai/SampleClock Too Fast

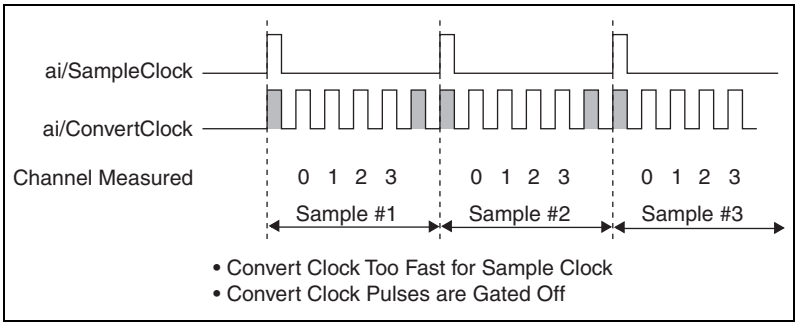


Figure 4-19. ai/ConvertClock Too Fast

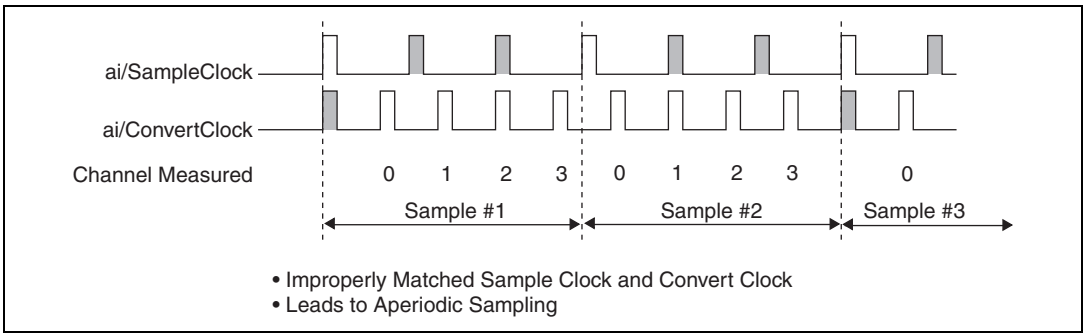


Figure 4-20. ai/SampleClock and ai/ConvertClock Improperly Matched

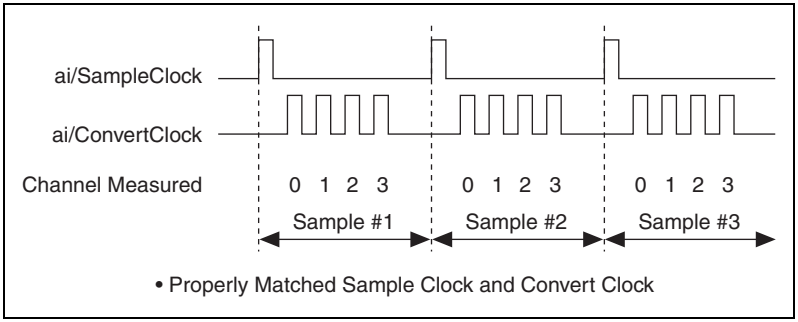


Figure 4-21. ai/SampleClock and ai/ConvertClock Properly Matched

It is also possible to use a single external signal to drive both ai/SampleClock and ai/ConvertClock at the same time. In this mode, each tick of the external clock will cause a conversion on the ADC. Figure 4-22 shows this timing relationship.

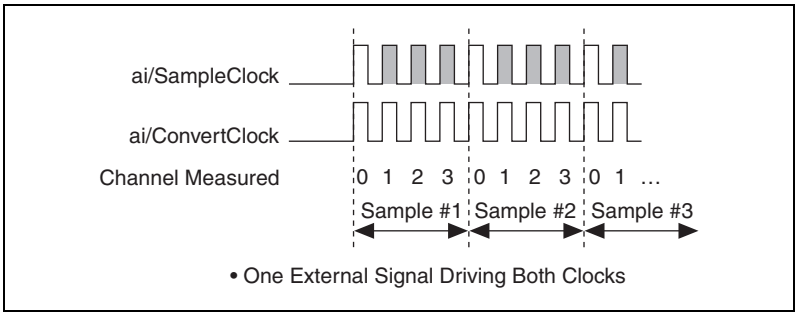


Figure 4-22. Single External Signal Driving ai/SampleClock and ai/ConvertClock Simultaneously

AI Convert Clock Timebase Signal

The AI Convert Clock Timebase (ai/ConvertClockTimebase) signal is divided down to provide on of the possible sources for ai/ConvertClock. Use one of the following signals as the source of ai/ConvertClockTimebase:

- ai/SampleClockTimebase
- 20 MHz Timebase

ai/ConvertClockTimebase is not available as an output on the I/O connector.

AI Hold Complete Event Signal

The AI Hold Complete Event (ai/HoldCompleteEvent) signal generates a pulse after each A/D conversion begins. You can route ai/HoldCompleteEvent out to any PFI <0..15> or RTSI <0..7> terminal.

The polarity of ai/HoldCompleteEvent is software-selectable, but is typically configured so that a low-to-high leading edge can clock external AI multiplexers indicating when the input signal has been sampled and can be removed.

AI Start Trigger Signal

Use the AI Start Trigger (ai/StartTrigger) signal to begin a measurement acquisition. A measurement acquisition consists of one or more samples. If you do not use triggers, begin a measurement with a software command. Once the acquisition begins, configure the acquisition to stop:

- When a certain number of points are sampled (in finite mode)
- After a hardware reference trigger (in finite mode)
- With a software command (in continuous mode)

An acquisition that uses a start trigger (but not a reference trigger) is sometimes referred to as a posttriggered acquisition.

Using a Digital Source

To use ai/StartTrigger with a digital source, specify a source and an edge. The source can be any of the following signals:

- PFI <0..15>
- RTSI <0..7>
- Counter *n* Internal Output
- PXI_STAR

The source also can be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

You also can specify whether the measurement acquisition begins on the rising edge or falling edge of ai/StartTrigger.

Using an Analog Source

When you use an analog trigger source, the acquisition begins on the first rising edge of the Analog Comparison Event signal.

Routing AI Start Trigger to an Output Terminal

You can route ai/StartTrigger out to any PFI <0..15> or RTSI <0..7> terminal.

The output is an active high pulse.

All PFI terminals are configured as inputs by default.

The device also uses ai/StartTrigger to initiate pretriggered DAQ operations. In most pretriggered applications, a software trigger generates ai/StartTrigger. Refer to the *AI Reference Trigger Signal* section for a complete description of the use of ai/StartTrigger and ai/ReferenceTrigger in a pretriggered DAQ operation.

AI Reference Trigger Signal

Use a reference trigger (ai/ReferenceTrigger) signal to stop a measurement acquisition. To use a reference trigger, specify a buffer of finite size and a number of pretrigger samples (samples that occur before the reference trigger). The number of posttrigger samples (samples that occur after the reference trigger) desired is the buffer size minus the number of pretrigger samples.

Once the acquisition begins, the DAQ device writes samples to the buffer. After the DAQ device captures the specified number of pretrigger samples, the DAQ device begins to look for the reference trigger condition. If the reference trigger condition occurs before the DAQ device captures the specified number of pretrigger samples, the DAQ device ignores the condition.

If the buffer becomes full, the DAQ device continuously discards the oldest samples in the buffer to make space for the next sample. This data can be accessed (with some limitations) before the DAQ device discards it. Refer to the KnowledgeBase document, *Can a Pretriggered Acquisition be Continuous?*, for more information. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rdcanq`.

When the reference trigger occurs, the DAQ device continues to write samples to the buffer until the buffer contains the number of posttrigger samples desired. Figure 4-23 shows the final buffer.

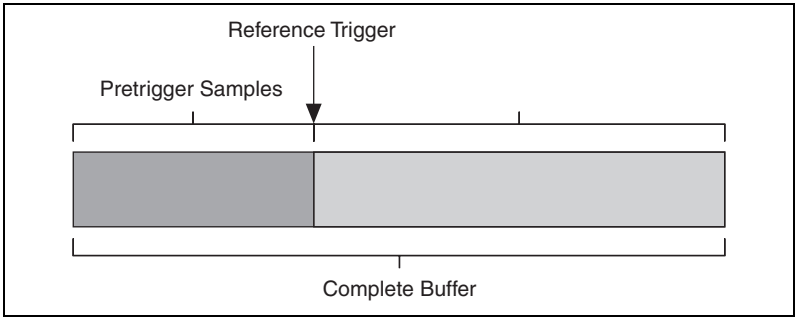


Figure 4-23. Reference Trigger Final Buffer

Using a Digital Source

To use ai/ReferenceTrigger with a digital source, specify a source and an edge. The source can be any of the following signals:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR

The source also can be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

You also can specify whether the measurement acquisition stops on the rising edge or falling edge of ai/ReferenceTrigger.

Using an Analog Source

When you use an analog trigger source, the acquisition stops on the first rising edge of the Analog Comparison Event signal.

Routing AI Reference Trigger Signal to an Output Terminal

You can route ai/ReferenceTrigger out to any PFI <0..15> or RTSI <0..7> terminal.

All PFI terminals are configured as inputs by default.

AI Pause Trigger Signal

You can use the AI Pause Trigger (ai/PauseTrigger) signal to pause and resume a measurement acquisition. The internal sample clock pauses while the external trigger signal is active and resumes when the signal is inactive. You can program the active level of the pause trigger to be high or low.

Using a Digital Source

To use ai/SampleClock, specify a source and a polarity. The source can be any of the following signals:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR

The source also can be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Using an Analog Source

When you use an analog trigger source, the internal sample clock pauses when the Analog Comparison Event signal is low and resumes when the signal goes high (or vice versa).

Routing AI Pause Trigger Signal to an Output Terminal

You can route ai/PauseTrigger out to RTSI <0..7>.

Note Pause triggers are only sensitive to the level of the source, not the edge.

Getting Started with AI Applications in Software

You can use the M Series device in the following analog input applications.

- Single-point analog input
- Finite analog input
- Continuous analog input

You can perform these applications through DMA, interrupt, or programmed I/O data transfer mechanisms. Some of the applications also use start, reference, and pause triggers.

Note For more information about programming analog input applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

5

Analog Output

Many M Series devices have analog output functionality. M Series devices that support analog output have either two or four AO channels that are controlled by a single clock and are capable of waveform generation. Refer to Appendix A, *Device-Specific Information*, for information about the capabilities of your device.

Figure 5-1 shows the analog output circuitry of M Series devices.

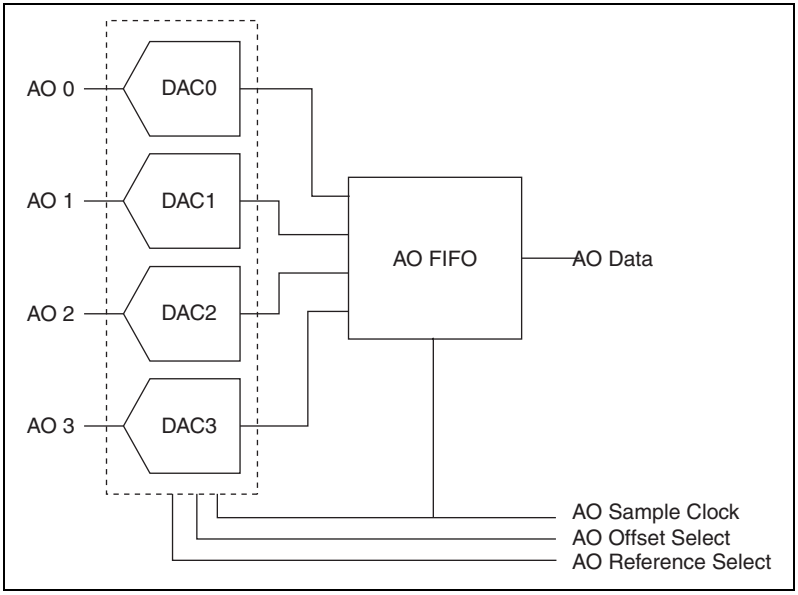


Figure 5-1. M Series Analog Output Circuitry

The main blocks featured in the M Series analog output circuitry are as follows:

- **DACs**—Digital-to-analog converters (DACs) convert digital codes to analog voltages.
- **AO FIFO**—The AO FIFO enables analog output waveform generation. It is a first-in-first-out (FIFO) memory buffer between the computer and the DACs. It allows you to download the points of a waveform to your M Series device without host computer interaction.

- **AO Sample Clock**—The AO Sample Clock signal reads a sample from the DAC FIFO and generates the AO voltage.
- **AO Offset and AO Reference Selection**—AO offset and AO reference selection signals allow you to change the range of the analog outputs.

AO Offset and AO Reference Selection

AO offset and AO reference selection allow you to set the AO range. The AO range describes the set of voltages the device can generate. The digital codes of the DAC are spread evenly across the AO range. So, if the range is smaller, the AO has better resolution; that is, the voltage output difference between two consecutive codes is smaller. Therefore, the AO is more accurate.

The AO range of a device is all of the voltages between:

(AO Offset – AO Reference) and (AO Offset + AO Reference)

The possible settings for AO reference depend on the device model. For models not described below, refer to the specifications for your device.

(NI 622*x* Devices) On NI 622*x* devices, the AO offset is always 0 V (AO GND). The AO reference is always 10 V. So, for NI 622*x* devices, the AO Range = ±10 V.

(NI 625*x* Devices) On NI 625*x* devices, the AO offset is always 0 V (AO GND). The AO reference of each analog output (AO <0..3>) can be individually set to one of the following:

- ±10 V
- ±5 V
- ±APFI <0..1>

You can connect an external signal to APFI <0..1> to provide the AO reference. The AO reference can be a positive or negative voltage. If AO reference is a negative voltage, the polarity of the AO output is inverted. The valid ranges of APFI <0..1> are listed in the device specifications.

You can use one of the AO <0..3> signals to be the AO reference for a different AO signal. However, you must externally connect this channel to APFI 0 or APFI 1.

(NI 628*x* Devices) On NI 628*x* devices, the AO offset of each analog output can be individually set to one of the following:

- 0 V (AO GND)
- 5 V
- APFI <0..1>
- AO <0..3>

You can connect an external signal to APFI <0..1> to provide the AO offset.

You can route the output of one of the AO <0..3> signals to be the AO offset for a different AO <0..3> signal. For example, AO 0 can be routed to be the AO offset of AO 1. This route is done on the device; no external connections are required.

You cannot route an AO channel to be its own offset.

On NI 628*x* devices, the AO reference of each analog output can be individually set to one of the following:

- ±10 V
- ±5 V
- ±APFI <0..1>
- ±AO <0..3>

You can connect an external signal to APFI <0..1> to provide the AO reference.

You can route the output of one of the AO <0..3> signals to be the AO reference for a different AO <0..3> signal. For example, AO 0 can be routed to be the AO reference of AO 1. This route is done on the device; no external connections are required.

You cannot route an AO channel to be its own reference.

The AO reference can be a positive or negative voltage. If AO reference is a negative voltage, the polarity of the AO output is inverted.

Minimizing Glitches on the Output Signal

When you use a DAC to generate a waveform, you may observe glitches on the output signal. These glitches are normal; when a DAC switches from one voltage to another, it produces glitches due to released charges. The largest glitches occur when the most significant bit of the DAC code changes. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal. Visit `ni.com/support` for more information about minimizing glitches.

Analog Output Data Generation Methods

When performing an analog output operation, you either can perform software-timed or hardware-timed generations. Hardware-timed generations can be non-buffered or buffered.

Software-Timed Generations

With a software-timed generation, software controls the rate at which data is generated. Software sends a separate command to the hardware to initiate each DAC conversion. In NI-DAQmx, software-timed generations are referred to as on-demand timing. Software-timed generations are also referred to as immediate or static operations. They are typically used for writing a single value out, such as a constant DC voltage.

Hardware-Timed Generations

With a hardware-timed generation, a digital hardware signal controls the rate of the generation. This signal can be generated internally on your device or provided externally.

Hardware-timed generations have several advantages over software-timed acquisitions:

- The time between samples can be much shorter.
- The timing between samples can be deterministic.
- Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or non-buffered. A buffer is a temporary storage in computer memory for to-be-generated samples.

Non-Buffered

In non-buffered acquisitions, data is written directly to the DACs on the device. Typically, hardware-timed, non-buffered operations are used to write single samples with good latency and known time increments between them.

Buffered

In a buffered acquisition, data is moved from a PC buffer to the DAQ device's onboard FIFO using DMA or interrupts for NI PCI/PCIe/PXI/PXIe devices or USB Signal Streams for USB devices before it is written to the DACs one sample at a time. Buffered acquisitions typically allow for much faster transfer rates than non-buffered acquisitions because data is moved in large blocks, rather than one point at a time.

One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous.

Finite sample mode generation refers to the generation of a specific, predetermined number of data samples. Once the specified number of samples has been written out, the generation stops.

Continuous generation refers to the generation of an unspecified number of samples. Instead of generating a set number of data samples and stopping, a continuous generation continues until you stop the operation. There are several different methods of continuous generation that control what data is written. These methods are regeneration, FIFO regeneration and non-regeneration modes.

Regeneration is the repetition of the data that is already in the buffer. Standard regeneration is when data from the PC buffer is continually downloaded to the FIFO to be written out. New data can be written to the PC buffer at any time without disrupting the output.

With FIFO regeneration, the entire buffer is downloaded to the FIFO and regenerated from there. Once the data is downloaded, new data cannot be written to the FIFO. To use FIFO regeneration, the entire buffer must fit within the FIFO size. The advantage of using FIFO regeneration is that it does not require communication with the main host memory once the operation is started, thereby preventing any problems that may occur due to excessive bus traffic.

With non-regeneration, old data will not be repeated. New data must be continually written to the buffer. If the program does not write new data to the buffer at a fast enough rate to keep up with the generation, the buffer will underflow and cause an error.

Analog Output Triggering

Analog output supports two different triggering actions:

- Start trigger
- Pause trigger

An analog or digital trigger can initiate these actions. All M Series devices support digital triggering, but some do not support analog triggering. To find your device's triggering options, refer to the specifications document for your device. Refer to the *AO Start Trigger Signal* and *AO Pause Trigger Signal* sections for more information about these triggering actions.

Connecting Analog Output Signals

AO <0..3> are the voltage output signals for AO channels 0, 1, 2, and 3. AO GND is the ground reference for AO <0..3>.

Figure 5-2 shows how to make AO connections to the device.

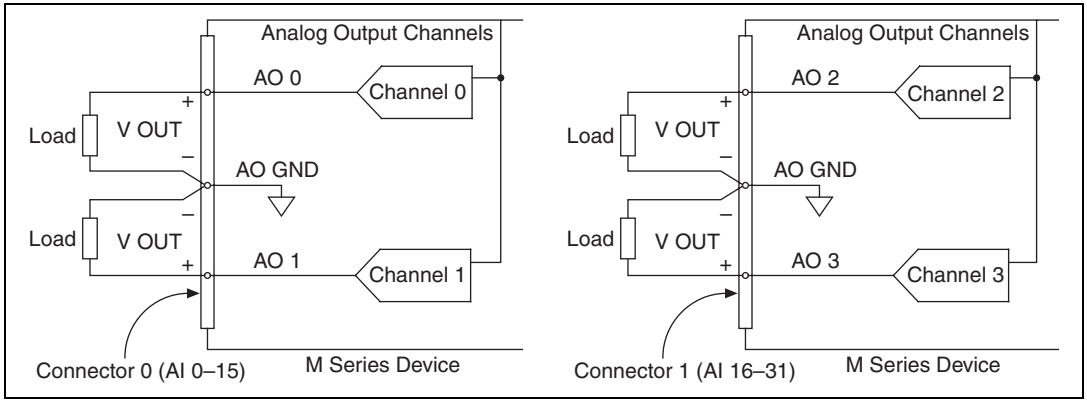


Figure 5-2. Analog Output Connections

Analog Output Timing Signals

Figure 5-3 summarizes all of the timing options provided by the analog output timing engine.

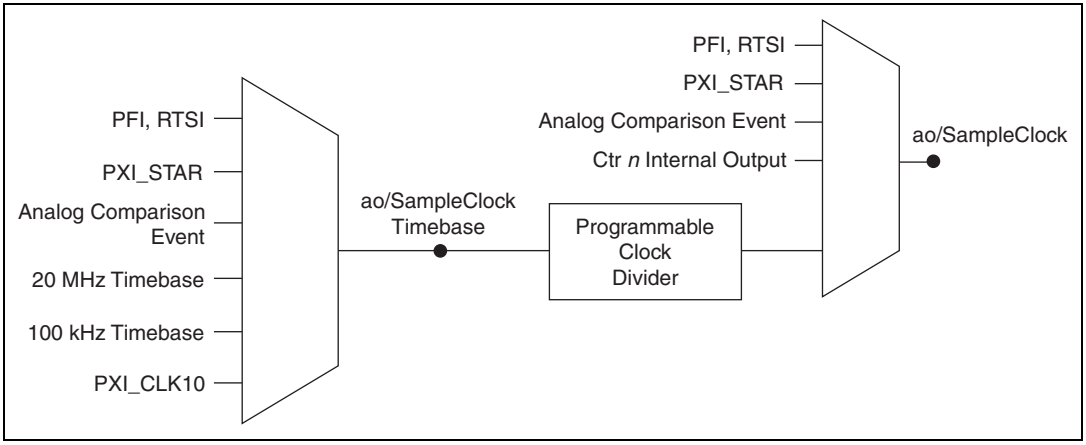


Figure 5-3. Analog Output Timing Options

M Series devices feature the following AO (waveform generation) timing signals.

- AO Start Trigger Signal
- AO Pause Trigger Signal
- AO Sample Clock Signal
- AO Sample Clock Timebase Signal

AO Start Trigger Signal

Use the AO Start Trigger (ao/StartTrigger) signal to initiate a waveform generation. If you do not use triggers, you can begin a generation with a software command.

Using a Digital Source

To use ao/StartTrigger, specify a source and an edge. The source can be one of the following signals:

- A pulse initiated by host software
- PFI <0..15>
- RTSI <0..7>

- ai/ReferenceTrigger
- ai/StartTrigger
- PXI_STAR

The source also can be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

You also can specify whether the waveform generation begins on the rising edge or falling edge of ao/StartTrigger.

Using an Analog Source

When you use an analog trigger source, the waveform generation begins on the first rising edge of the Analog Comparison Event signal. Refer to the *Triggering with an Analog Source* section of Chapter 11, *Triggering*, for more information.

Routing AO Start Trigger Signal to an Output Terminal

You can route ao/StartTrigger out to any PFI <0..15> or RTSI <0..7> terminal.

The output is an active high pulse.

PFI terminals are configured as inputs by default.

AO Pause Trigger Signal

Use the AO Pause trigger signal (ao/PauseTrigger) to mask off samples in a DAQ sequence. That is, when ao/PauseTrigger is active, no samples occur.

ao/PauseTrigger does not stop a sample that is in progress. The pause does not take effect until the beginning of the next sample.

When you generate analog output signals, the generation pauses as soon as the pause trigger is asserted. If the source of your sample clock is the onboard clock, the generation resumes as soon as the pause trigger is deasserted, as shown in Figure 5-4.

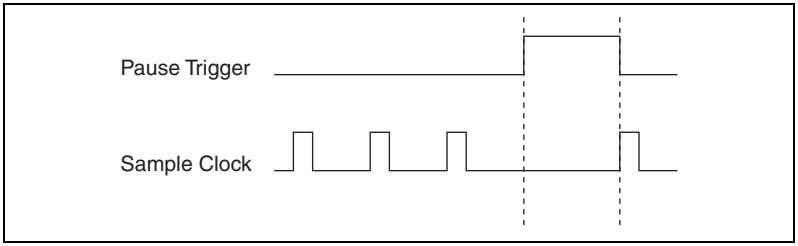


Figure 5-4. ao/PauseTrigger with the Onboard Clock Source

If you are using any signal other than the onboard clock as the source of your sample clock, the generation resumes as soon as the pause trigger is deasserted and another edge of the sample clock is received, as shown in Figure 5-5.

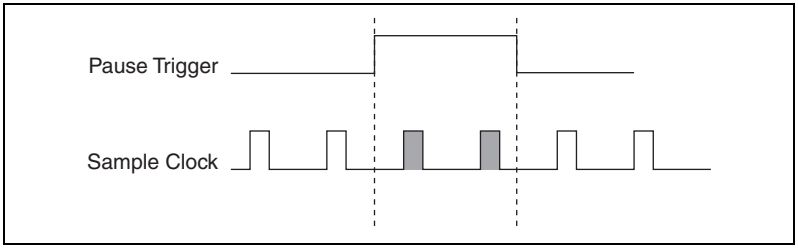


Figure 5-5. ao/PauseTrigger with Other Signal Source

Using a Digital Source

To use ao/PauseTrigger, specify a source and a polarity. The source can be one of the following signals:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR

The source also can be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

You also can specify whether the samples are paused when ao/PauseTrigger is at a logic high or low level.

Using an Analog Source

When you use an analog trigger source, the samples are paused when the Analog Comparison Event signal is at a high level. Refer to the *Triggering with an Analog Source* section of Chapter 11, *Triggering*, for more information.

Routing AO Pause Trigger Signal to an Output Terminal

You can route ao/PauseTrigger out to RTSI <0..7>.

AO Sample Clock Signal

Use the AO Sample Clock (ao/SampleClock) signal to initiate AO samples. Each sample updates the outputs of all of the DACs. You can specify an internal or external source for ao/SampleClock. You also can specify whether the DAC update begins on the rising edge or falling edge of ao/SampleClock.

Using an Internal Source

One of the following internal signals can drive ao/SampleClock.

- AO Sample Clock Timebase (divided down)
- Counter *n* Internal Output

A programmable internal counter divides down the AO Sample Clock Timebase signal.

Using an External Source

Use one of the following external signals as the source of ao/SampleClock:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR
- Analog Comparison Event (an analog trigger)

Routing AO Sample Clock Signal to an Output Terminal

You can route ao/SampleClock (as an active low signal) out to any PFI <0..15> or RTSI <0..7> terminal.

Other Timing Requirements

A counter on your device internally generates ao/SampleClock unless you select some external source. ao/StartTrigger starts the counter and either the software or hardware can stop it once a finite generation completes. When using an internally generated ao/SampleClock, you also can specify a configurable delay from ao/StartTrigger to the first ao/SampleClock pulse. By default, this delay is two ticks of ao/SampleClockTimebase.

Figure 5-6 shows the relationship of ao/SampleClock to ao/StartTrigger.

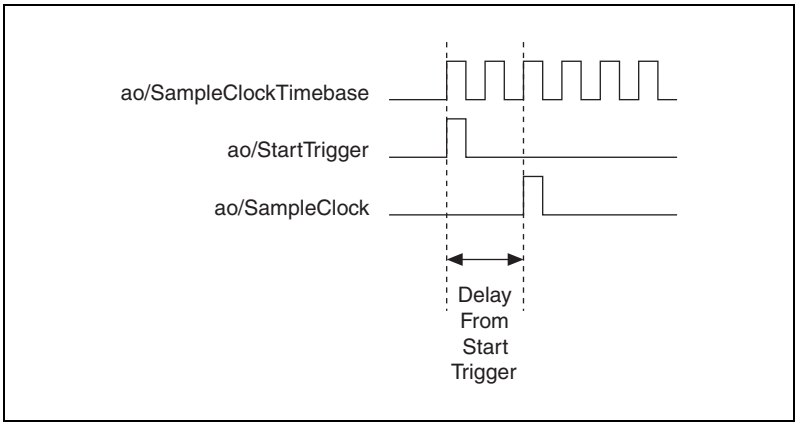


Figure 5-6. ao/SampleClock and ao/StartTrigger

AO Sample Clock Timebase Signal

The AO Sample Clock Timebase (ao/SampleClockTimebase) signal is divided down to provide a source for ao/SampleClock.

You can route any of the following signals to be the AO Sample Clock Timebase (ao/SampleClockTimebase) signal:

- 20 MHz Timebase
- 100 kHz Timebase
- PXI_CLK10
- PFI <0..15>

- RTSI <0..7>
- PXI_STAR
- Analog Comparison Event (an analog trigger)

ao/SampleClockTimebase is not available as an output on the I/O connector.

You might use ao/SampleClockTimebase if you want to use an external sample clock signal, but need to divide the signal down. If you want to use an external sample clock signal, but do not need to divide the signal, then you should use ao/SampleClock rather than ao/SampleClockTimebase.

Getting Started with AO Applications in Software

You can use an M Series device in the following analog output applications.

- Single-point (on-demand) generation
- Finite generation
- Continuous generation
- Waveform generation

You can perform these generations through programmed I/O, interrupt, or DMA data transfer mechanisms. Some of the applications also use start triggers and pause triggers.

Note For more information about programming analog output applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

6

Digital I/O

M Series devices contain up to 32 lines of bidirectional DIO signals on Port 0. In addition, M Series devices have up to 16 PFI signals that can function as static DIO signals.

M Series devices support the following DIO features on Port 0:

- Up to 32 lines of DIO
- Direction and function of each terminal individually controllable
- Static digital input and output
- High-speed digital waveform generation
- High-speed digital waveform acquisition
- DI change detection trigger/interrupt

Figure 6-1 shows the circuitry of one DIO line. Each DIO line is similar. The following sections provide information about the various parts of the DIO circuit.

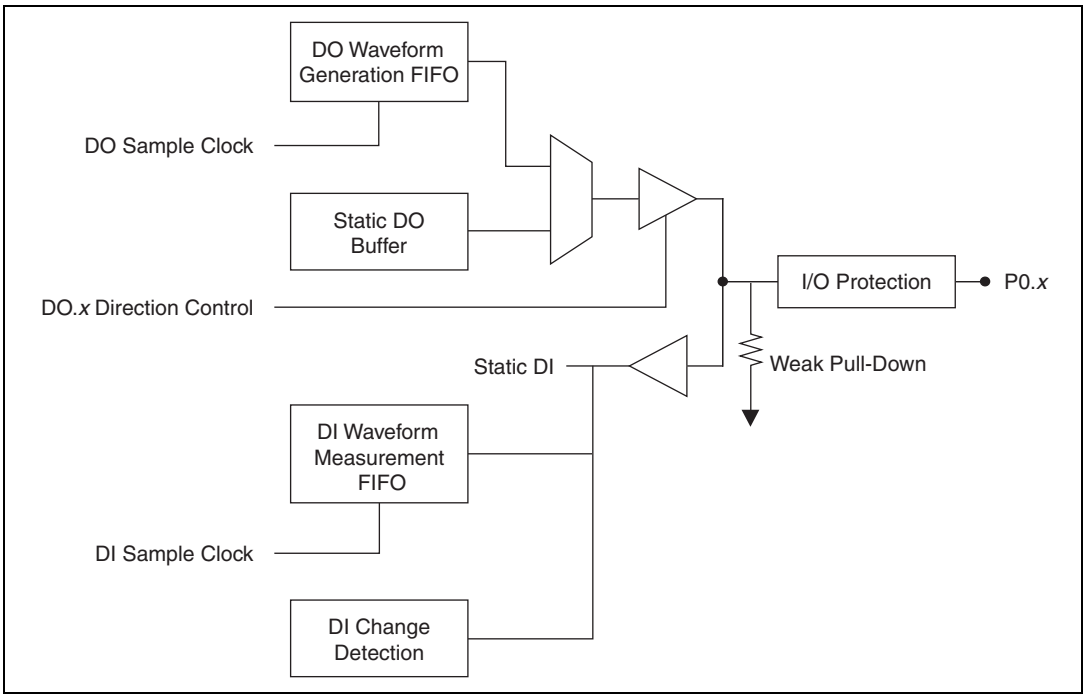


Figure 6-1. M Series Digital I/O Circuitry

The DIO terminals are named P0.<0..31> on the M Series device I/O connector.

The voltage input and output levels and the current drive levels of the DIO lines are listed in the specifications of your device.

Static DIO

Each of the M Series DIO lines can be used as a static DI or DO line. You can use static DIO lines to monitor or control digital signals. Each DIO can be individually configured as a digital input (DI) or digital output (DO).

All samples of static DI lines and updates of DO lines are software-timed.

P0.6 and P0.7 on 68-pin M Series devices also can control the up/down input of general-purpose counters 0 and 1, respectively. However, it is recommended that you use PFI signals to control the up/down input of the counters. The up/down control signals, Counter 0 Up_Down and Counter 1 Up_Down, are input-only and do not affect the operation of the DIO lines.

Digital Waveform Triggering

M Series devices do not have an independent DI or DO Start Trigger for digital waveform acquisition or generation. To trigger a DI or DO operation, first select a signal to be the source of DI Sample Clock or DO Sample Clock. Then, generate a trigger that initiates pulses on the source signal. The method for generating this trigger depends on which signal is the source of DI Sample Clock or DO Sample Clock.

For example, consider the case where you are using AI Sample Clock as the source of DI Sample Clock. To initiate pulses on AI Sample Clock (and therefore on DI Sample Clock), you use AI Start Trigger to trigger the start of an AI operation. The AI Start Trigger causes the M Series device to begin generating AI Sample clock pulses, which in turn generates DI Sample clock pulses, as shown in Figure 6-2.

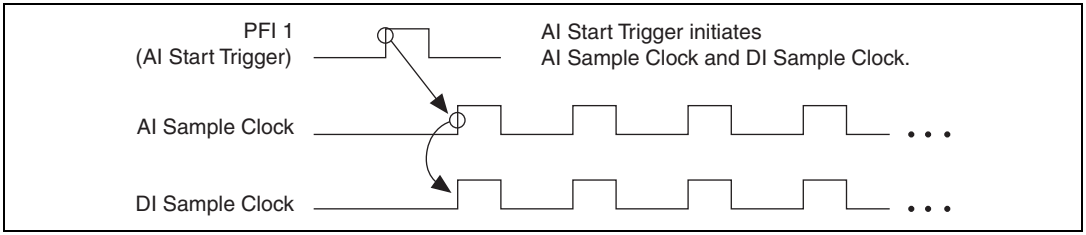


Figure 6-2. Digital Waveform Triggering

Similarly, if you are using AO Sample Clock as the source of DI Sample Clock, then AO Start Trigger initiates both AO and DI operations.

If you are using a Counter output as the source of DI Sample Clock, the counter's start trigger, enables the counter which drives DI Sample Clock.

If you are using an external signal (such as PFI *x*) as the source for DI Sample Clock or DO Sample Clock, you must trigger that external signal.

Digital Waveform Acquisition

You can acquire digital waveforms on the Port 0 DIO lines. The DI waveform acquisition FIFO stores the digital samples. M Series devices have a DMA controller dedicated to moving data from the DI waveform acquisition FIFO to system memory. The DAQ device samples the DIO lines on each rising or falling edge of a clock signal, di/SampleClock.

You can configure each DIO line to be an output, a static input, or a digital waveform acquisition input.

DI Sample Clock Signal

Use the DI Sample Clock (di/SampleClock) signal to sample the P0.<0..31> terminals and store the result in the DI waveform acquisition FIFO. M Series devices do not have the ability to divide down a timebase to produce an internal DI Sample Clock for digital waveform acquisition. Therefore, you must route an external signal or one of many internal signals from another subsystem to be the DI Sample Clock. For example, you can correlate digital and analog samples in time by sharing your AI Sample Clock or AO Sample Clock as the source of your DI Sample Clock. To sample a digital signal independent of an AI, AO, or DO operation, you can configure a counter to generate the desired DI Sample Clock or use an external signal as the source of the clock.

If the DAQ device receives a di/SampleClock when the FIFO is full, it reports an overflow error to the host software.

Using an Internal Source

To use di/SampleClock with an internal source, specify the signal source and the polarity of the signal. The source can be any of the following signals:

- AI Sample Clock
- AI Convert Clock
- AO Sample Clock
- Counter *n* Internal Output
- Frequency Output
- DI Change Detection Output

Several other internal signals can be routed to di/SampleClock through RTSI. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Using an External Source

You can route any of the following signals as di/SampleClock:

- PFI <0..15>
- RTSI <0..7>

- PXI_STAR
- Analog Comparison Event (an analog trigger)

You can sample data on the rising or falling edge of di/SampleClock.

Routing DI Sample Clock to an Output Terminal

You can route di/SampleClock out to any PFI terminal. The PFI circuitry inverts the polarity of di/SampleClock before driving the PFI terminal.

Digital Waveform Generation

You can generate digital waveforms on the Port 0 DIO lines. The DO waveform generation FIFO stores the digital samples. M Series devices have a DMA controller dedicated to moving data from the system memory to the DO waveform generation FIFO. The DAQ device moves samples from the FIFO to the DIO terminals on each rising or falling edge of a clock signal, do/SampleClock. You can configure each DIO signal to be an input, a static output, or a digital waveform generation output.

The FIFO supports a retransmit mode. In the retransmit mode, after all the samples in the FIFO have been clocked out, the FIFO begins outputting all of the samples again in the same order. For example, if the FIFO contains five samples, the pattern generated consists of sample #1, #2, #3, #4, #5, #1, #2, #3, #4, #5, #1, and so on.

DO Sample Clock Signal

Use the DO Sample Clock (do/SampleClock) signal to update the DO terminals with the next sample from the DO waveform generation FIFO. M Series devices do not have the ability to divide down a timebase to produce an internal DO Sample Clock for digital waveform generation. Therefore, you must route an external signal or one of many internal signals from another subsystem to be the DO Sample Clock. For example, you can correlate digital and analog samples in time by sharing your AI Sample Clock or AO Sample Clock as the source of your DO Sample Clock. To generate digital data independent of an AI, AO, or DI operation, you can configure a counter to generate the desired DO Sample Clock or use an external signal as the source of the clock.

If the DAQ device receives a do/SampleClock when the FIFO is empty, the DAQ device reports an underflow error to the host software.

Using an Internal Source

To use do/SampleClock with an internal source, specify the signal source and the polarity of the signal. The source can be any of the following signals:

- AI Sample Clock
- AI Convert Clock
- AO Sample Clock
- Counter *n* Internal Output
- Frequency Output
- DI Change Detection Output

Several other internal signals can be routed to do/SampleClock through RTSI. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information.

Using an External Source

You can route any of the following signals as do/SampleClock:

- PFI <0..15>
- RTSI <0..7>
- PXI_STAR
- Analog Comparison Event (an analog trigger)

You can generate samples on the rising or falling edge of do/SampleClock.

You must ensure that the time between two active edges of do/SampleClock is not too short. If the time is too short, the DO waveform generation FIFO is not able to read the next sample fast enough. The DAQ device reports an overrun error to the host software.

Routing DO Sample Clock to an Output Terminal

You can route do/SampleClock out to any PFI terminal. The PFI circuitry inverts the polarity of do/SampleClock before driving the PFI terminal.

I/O Protection

Each DIO and PFI signal is protected against overvoltage, undervoltage, and overcurrent conditions as well as ESD events. However, you should avoid these fault conditions by following these guidelines.

- If you configure a PFI or DIO line as an output, do not connect it to any external signal source, ground, or power supply.
- If you configure a PFI or DIO line as an output, understand the current requirements of the load connected to these signals. Do not exceed the specified current output limits of the DAQ device. NI has several signal conditioning solutions for digital applications requiring high current drive.
- If you configure a PFI or DIO line as an input, do not drive the line with voltages outside of its normal operating range. The PFI or DIO lines have a smaller operating range than the AI signals.
- Treat the DAQ device as you would treat any static sensitive device. Always properly ground yourself and the equipment when handling the DAQ device or connecting to it.

Programmable Power-Up States

At system startup and reset, the hardware sets all PFI and DIO lines to high-impedance inputs by default. The DAQ device does not drive the signal high or low. Each line has a weak pull-down resistor connected to it, as described in the specifications document for your device.

NI-DAQmx 7.4 and later supports programmable power-up states for PFI and DIO lines. Software can program any value at power up to the P0, P1, or P2 lines. The PFI and DIO lines can be set as:

- A high-impedance input with a weak pull-down resistor (default)
- An output driving a 0
- An output driving a 1

Refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information about setting power-up states in NI-DAQmx or MAX.

Note When using your M Series device to control an SCXI chassis, DIO lines 0, 1, 2, and 4 are used as communication lines and must be left to power-up in the default high-impedance state to avoid potential damage to these signals.

DI Change Detection

You can configure the DAQ device to detect changes in the DIO signals. Figure 6-3 shows a block diagram of the DIO change detection circuitry.

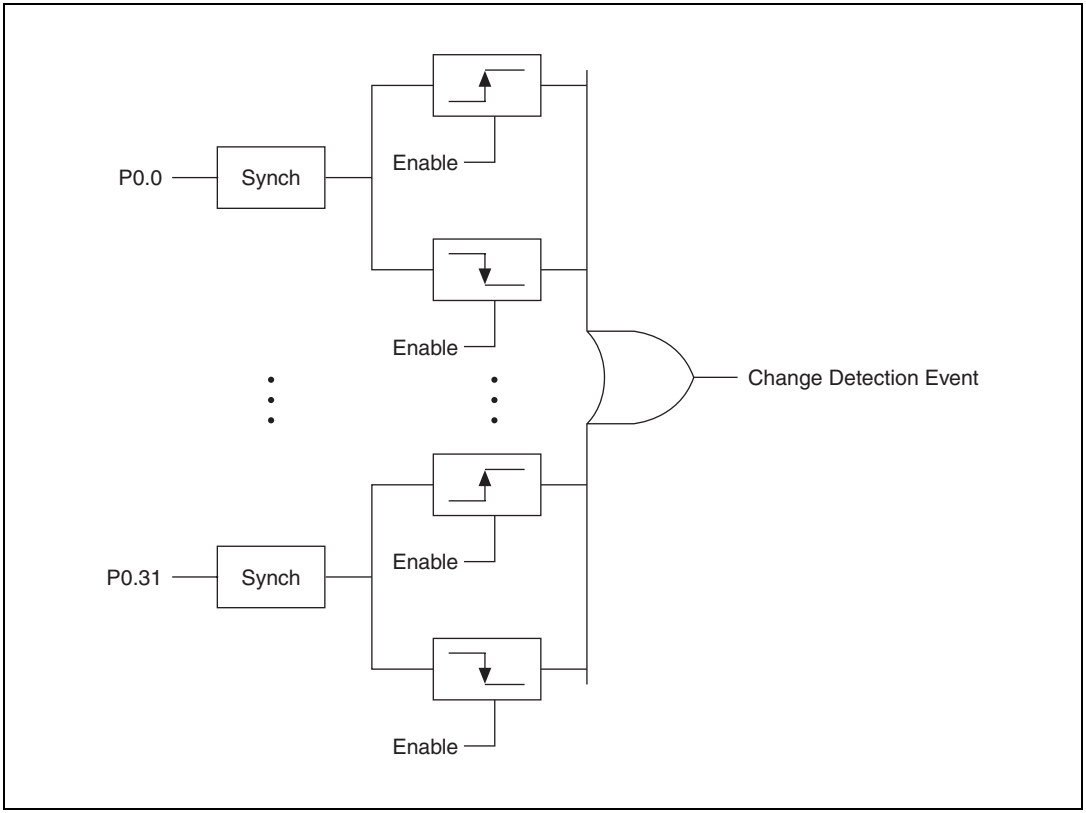


Figure 6-3. DI Change Detection

Note DI change detection is supported by NI-DAQmx 8.0 and later.

You can enable the DIO change detection circuitry to detect rising edges, falling edges, or either edge individually on each DIO line. The DAQ devices synchronize each DI signal to 80MHzTimebase, and then sends the signal to the change detectors. The circuitry ORs the output of all enabled change detectors from every DI signal. The result of this OR is the Change Detection Event signal.

The Change Detection Event signal can do the following:

- Drive any RTSI <0..7>, PFI <0..15>, or PXI_STAR signal
- Drive the DO Sample Clock or DI Sample Clock
- Generate an interrupt

The Change Detection Event signal also can be used to detect changes on digital output events.

Applications

The DIO change detection circuitry can interrupt a user program when one of several DIO signals changes state.

You also can use the output of the DIO change detection circuitry to trigger a DI or counter acquisition on the logical OR of several digital signals. To trigger on a single digital signal, refer to the *Triggering with a Digital Source* section of Chapter 11, *Triggering*. By routing the Change Detection Event signal to a counter, you also can capture the relative time between samples.

You also can use the Change Detection Event signal to trigger DO or counter generations.

Connecting Digital I/O Signals

The DIO signals, P0.<0..31>, P1.<0..7>, and P2.<0..7> are referenced to D GND. You can individually program each line as an input or output. Figure 6-4 shows P1.<0..3> configured for digital input and P1.<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states, such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices, such as the LED shown in the figure.

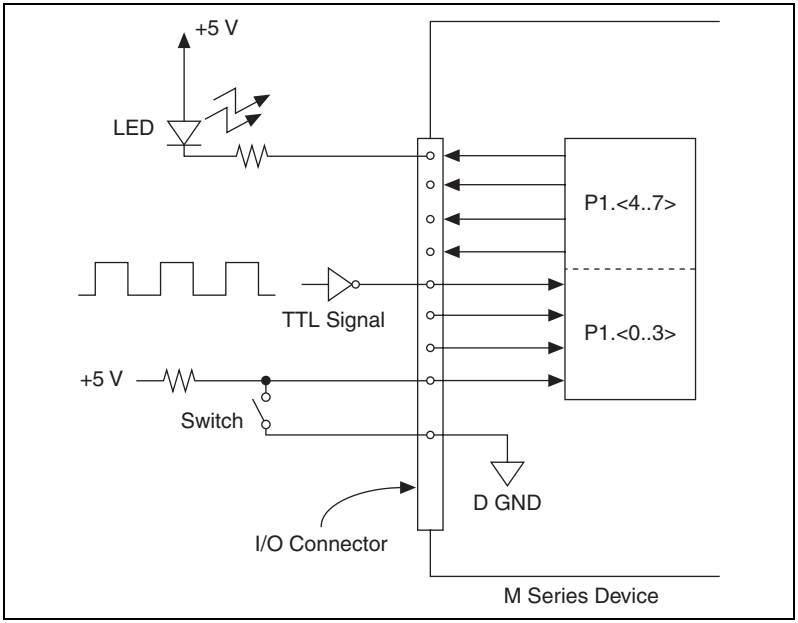


Figure 6-4. Digital I/O Connections

Caution Exceeding the maximum input voltage ratings, which are listed in the specifications document for each M Series device, can damage the DAQ device and the computer. NI is *not* liable for any damage resulting from such signal connections.

Getting Started with DIO Applications in Software

You can use the M Series device in the following digital I/O applications:

- Static digital input
- Static digital output
- Digital waveform generation
- Digital waveform acquisition
- DI change detection

Note For more information about programming digital I/O applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

7

Counters

M Series devices have two general-purpose 32-bit counter/timers and one frequency generator, as shown in Figure 7-1. The general-purpose counter/timers can be used for many measurement and pulse generation applications.

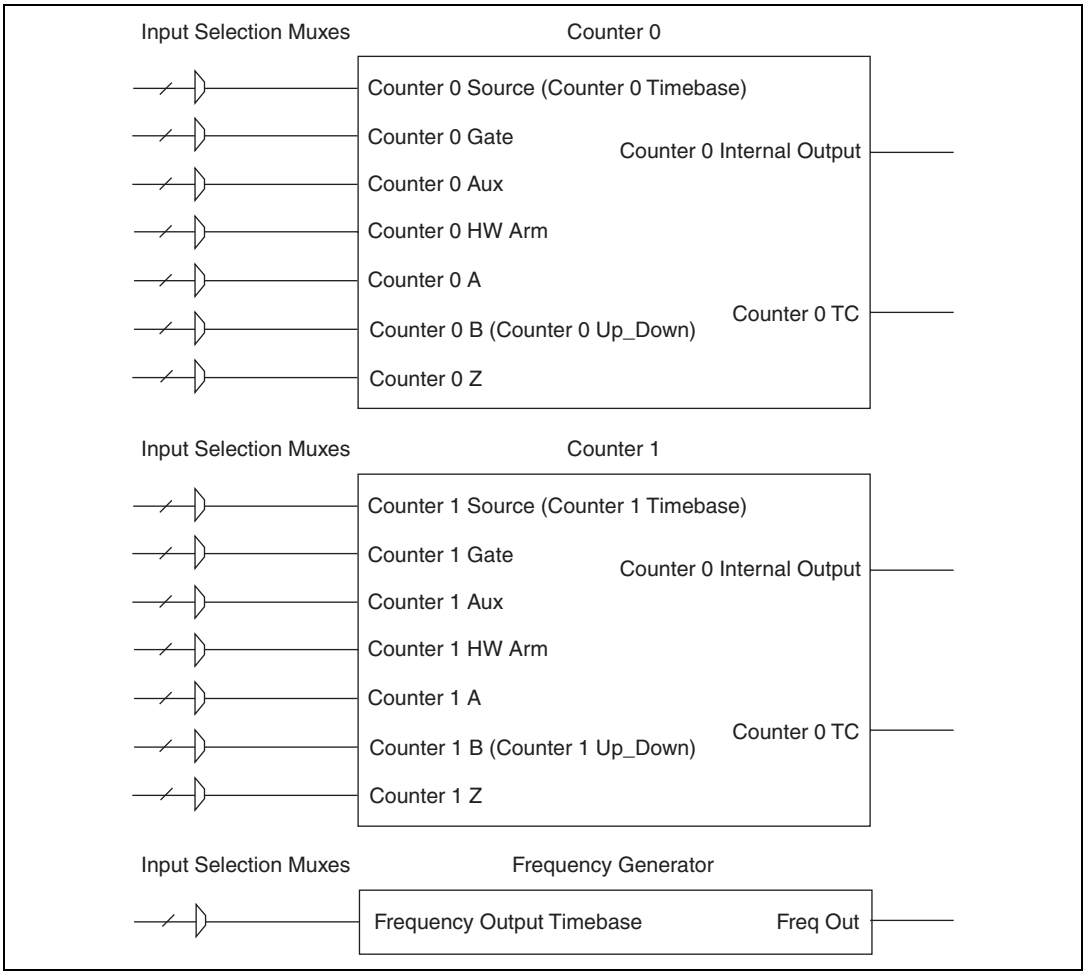


Figure 7-1. M Series Counters

The counters have seven input signals, although in most applications only a few inputs are used.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Counter Input Applications

Counting Edges

In edge counting applications, the counter counts edges on its Source after the counter is armed. You can configure the counter to count rising or falling edges on its Source input. You also can control the direction of counting (up or down).

The counter values can be read on demand or with a sample clock.

Single Point (On-Demand) Edge Counting

With single point (on-demand) edge counting, the counter counts the number of edges on the Source input after the counter is armed. *On-demand* refers to the fact that software can read the counter contents at any time without disturbing the counting process. Figure 7-2 shows an example of single point edge counting.

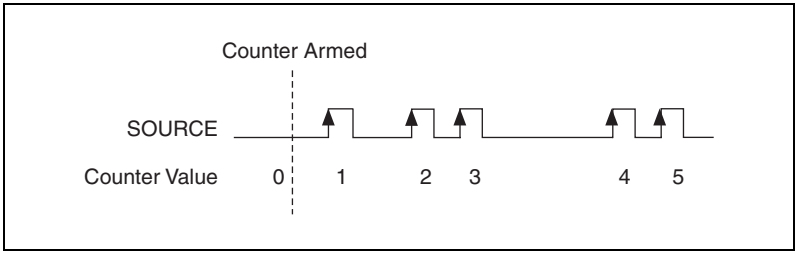


Figure 7-2. Single Point (On-Demand) Edge Counting

You also can use a pause trigger to pause (or gate) the counter. When the pause trigger is active, the counter ignores edges on its Source input. When the pause trigger is inactive, the counter counts edges normally.

You can route the pause trigger to the Gate input of the counter. You can configure the counter to pause counting when the pause trigger is high or when it is low. Figure 7-3 shows an example of on-demand edge counting with a pause trigger.

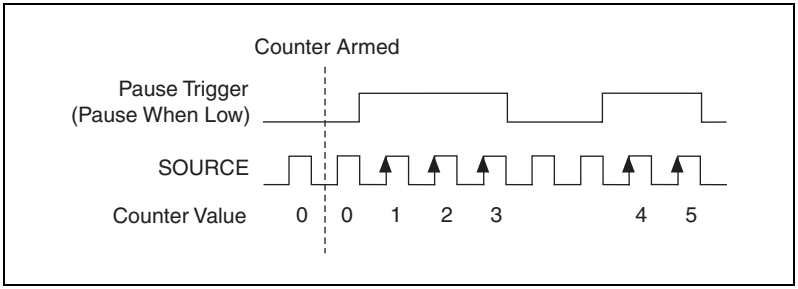


Figure 7-3. Single Point (On-Demand) Edge Counting with Pause Trigger

Buffered (Sample Clock) Edge Counting

With buffered edge counting (edge counting using a sample clock), the counter counts the number of edges on the Source input after the counter is armed. The value of the counter is sampled on each active edge of a sample clock. A DMA controller transfers the sampled values to host memory.

The count values returned are the cumulative counts since the counter armed event. That is, the sample clock does not reset the counter.

You can route the counter sample clock to the Gate input of the counter. You can configure the counter to sample on the rising or falling edge of the sample clock.

Figure 7-4 shows an example of buffered edge counting. Notice that counting begins when the counter is armed, which occurs before the first active edge on Gate.

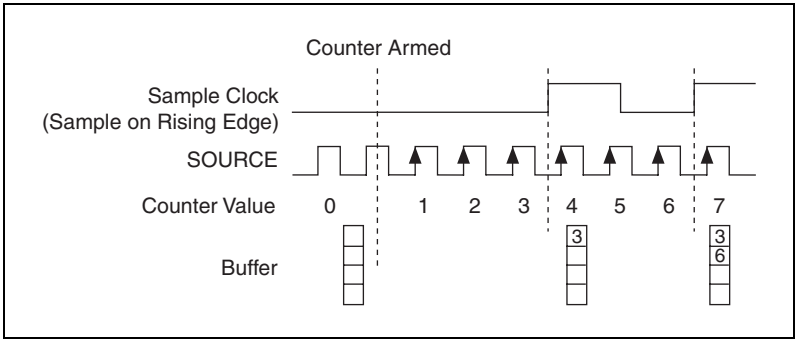


Figure 7-4. Buffered (Sample Clock) Edge Counting

Controlling the Direction of Counting

In edge counting applications, the counter can count up or down. You can configure the counter to do the following:

- Always count up
- Always count down
- Count up when the Counter *n* B input is high; count down when it is low

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Pulse-Width Measurement

In pulse-width measurements, the counter measures the width of a pulse on its Gate input signal. You can configure the counter to measure the width of high pulses or low pulses on the Gate signal.

You can route an internal or external periodic clock signal (with a known period) to the Source input of the counter. The counter counts the number of rising (or falling) edges on the Source signal while the pulse on the Gate signal is active.

You can calculate the pulse width by multiplying the period of the Source signal by the number of edges returned by the counter.

A pulse-width measurement will be accurate even if the counter is armed while a pulse train is in progress. If a counter is armed while the pulse is in the active state, it will wait for the next transition to the active state to begin the measurement.

Single Pulse-Width Measurement

With single pulse-width measurement, the counter counts the number of edges on the Source input while the Gate input remains active. When the Gate input goes inactive, the counter stores the count in a hardware save register and ignores other edges on the Gate and Source inputs. Software then reads the stored count.

Figure 7-5 shows an example of a single pulse-width measurement.

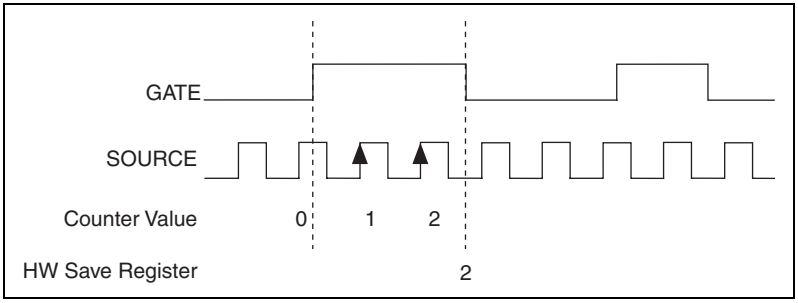


Figure 7-5. Single Pulse-Width Measurement

Buffered Pulse-Width Measurement

Buffered pulse-width measurement is similar to single pulse-width measurement, but buffered pulse-width measurement takes measurements over multiple pulses.

The counter counts the number of edges on the Source input while the Gate input remains active. On each trailing edge of the Gate signal, the counter stores the count in a hardware save register. A DMA controller transfers the stored values to host memory.

Figure 7-6 shows an example of a buffered pulse-width measurement.

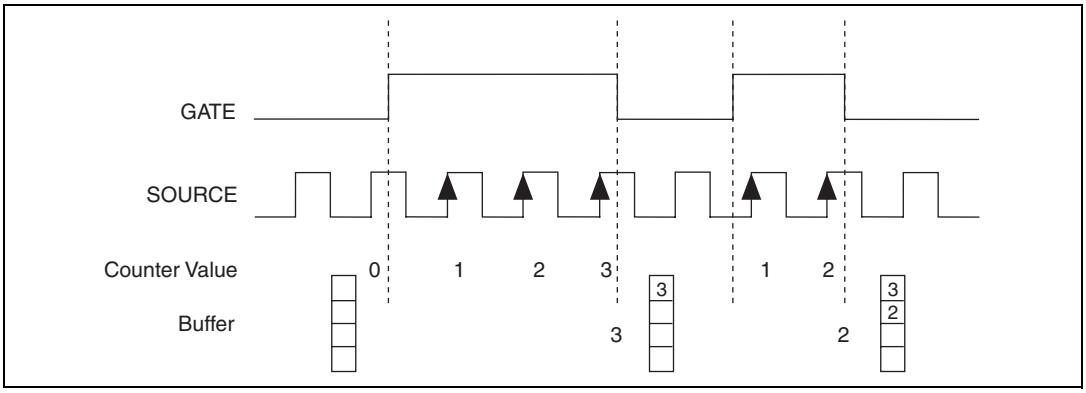


Figure 7-6. Buffered Pulse-Width Measurement

Note that if you are using an external signal as the Source, at least one Source pulse should occur between each active edge of the Gate signal. This condition ensures that correct values are returned by the counter. If

this condition is not met, consider using duplicate count prevention, described in the *Duplicate Count Prevention* section.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Period Measurement

In period measurements, the counter measures a period on its Gate input signal after the counter is armed. You can configure the counter to measure the period between two rising edges or two falling edges of the Gate input signal.

You can route an internal or external periodic clock signal (with a known period) to the Source input of the counter. The counter counts the number of rising (or falling) edges occurring on the Source input between the two active edges of the Gate signal.

You can calculate the period of the Gate input by multiplying the period of the Source signal by the number of edges returned by the counter.

Single Period Measurement

With single period measurement, the counter counts the number of rising (or falling) edges on the Source input occurring between two active edges of the Gate input. On the second active edge of the Gate input, the counter stores the count in a hardware save register and ignores other edges on the Gate and Source inputs. Software then reads the stored count.

Figure 7-7 shows an example of a single period measurement.

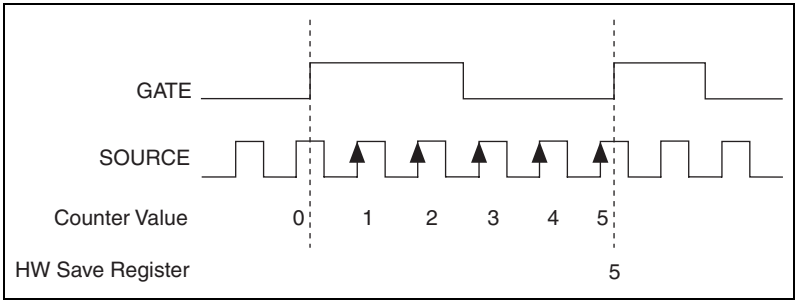


Figure 7-7. Single Period Measurement

Buffered Period Measurement

Buffered period measurement is similar to single period measurement, but buffered period measurement measures multiple periods.

The counter counts the number of rising (or falling) edges on the Source input between each pair of active edges on the Gate input. At the end of each period on the Gate signal, the counter stores the count in a hardware save register. A DMA controller transfers the stored values to host memory.

The counter begins when it is armed. The arm usually occurs in the middle of a period of the Gate input. So the first value stored in the hardware save register does not reflect a full period of the Gate input. In most applications, this first point should be discarded.

Figure 7-8 shows an example of a buffered period measurement.

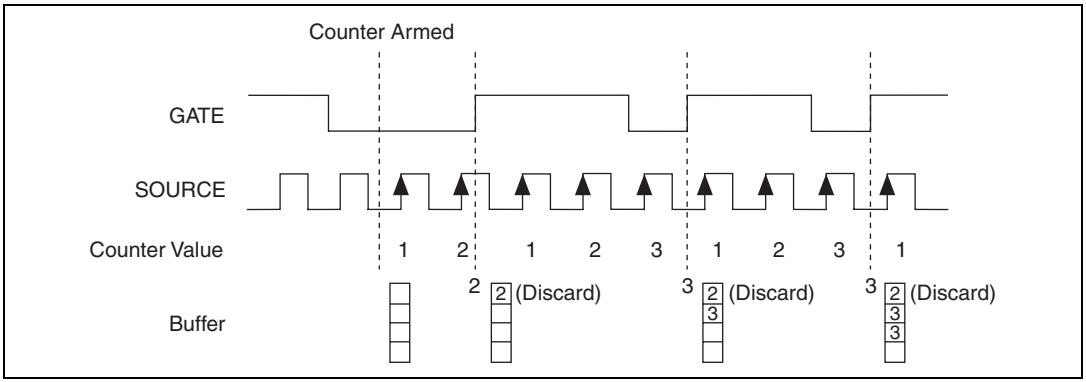


Figure 7-8. Buffered Period Measurement

Note that if you are using an external signal as the Source, at least one Source pulse should occur between each active edge of the Gate signal. This condition ensures that correct values are returned by the counter. If this condition is not met, consider using duplicate count prevention, described in the *Duplicate Count Prevention* section.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Semi-Period Measurement

In semi-period measurements, the counter measures a semi-period on its Gate input signal after the counter is armed. A semi-period is the time between any two consecutive edges on the Gate input.

You can route an internal or external periodic clock signal (with a known period) to the Source input of the counter. The counter counts the number of rising (or falling) edges occurring on the Source input between two edges of the Gate signal.

You can calculate the semi-period of the Gate input by multiplying the period of the Source signal by the number of edges returned by the counter.

Single Semi-Period Measurement

Single semi-period measurement is equivalent to single pulse-width measurement.

Buffered Semi-Period Measurement

In buffered semi-period measurement, on each edge of the Gate signal, the counter stores the count in a hardware save register. A DMA controller transfers the stored values to host memory.

The counter begins counting when it is armed. The arm usually occurs between edges on the Gate input. So the first value stored in the hardware save register does not reflect a full semi-period of the Gate input. In most applications, this first point should be discarded.

Figure 7-9 shows an example of a buffered semi-period measurement.

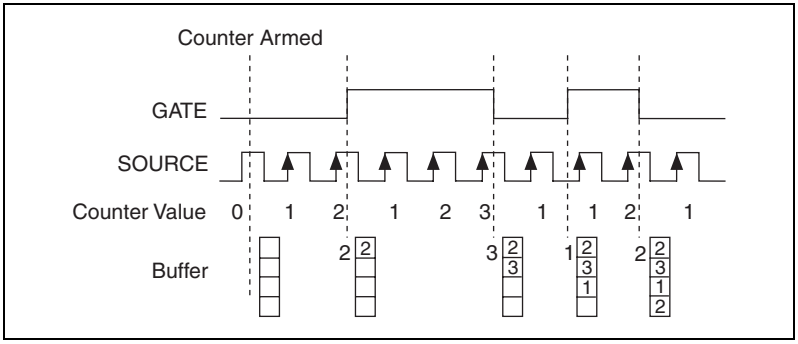


Figure 7-9. Buffered Semi-Period Measurement

Note that if you are using an external signal as the Source, at least one Source pulse should occur between each active edge of the Gate signal. This condition ensures that correct values are returned by the counter. If this condition is not met, consider using duplicate count prevention, described in the *Duplicate Count Prevention* section.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Frequency Measurement

You can use the counters to measure frequency in several different ways. You can choose one of the following methods depending on your application.

Method 1—Measure Low Frequency with One Counter

In this method, you measure one period of your signal using a known timebase. This method is good for low frequency signals.

You can route the signal to measure (F1) to the Gate of a counter. You can route a known timebase (Ft) to the Source of the counter. The known timebase can be 80MHzTimebase. For signals that might be slower than 0.02 Hz, use a slower known timebase.

You can configure the counter to measure one period of the gate signal. The frequency of F1 is the inverse of the period. Figure 7-10 illustrates this method.

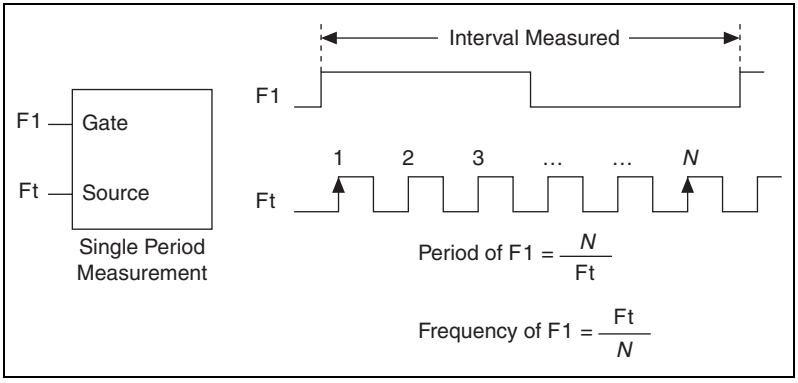


Figure 7-10. Method 1

Method 1b—Measure Low Frequency with One Counter (Averaged)

In this method, you measure several periods of your signal using a known timebase. This method is good for low to medium frequency signals.

You can route the signal to measure (F1) to the Gate of a counter. You can route a known timebase (Ft) to the Source of the counter. The known timebase can be 80MHzTimebase. For signals that might be slower than 0.02 Hz, use a slower known timebase.

You can configure the counter to make K + 1 buffered period measurements. Recall that the first period measurement in the buffer should be discarded.

Average the remaining K period measurements to determine the average period of F1. The frequency of F1 is the inverse of the average period. Figure 7-11 illustrates this method.

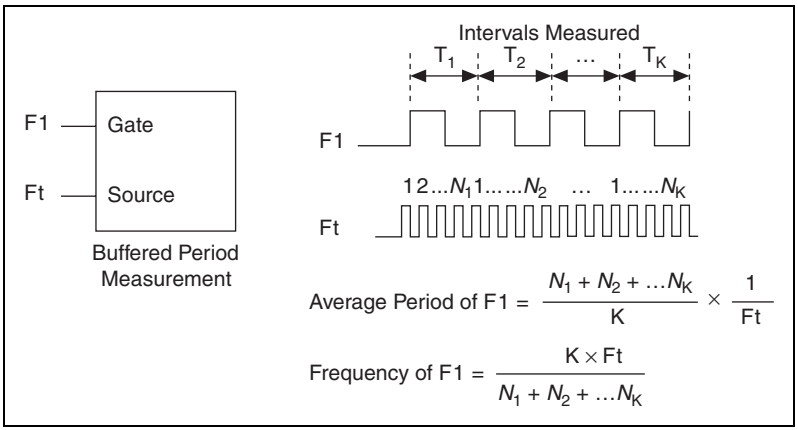


Figure 7-11. Method 1b

Method 2—Measure High Frequency with Two Counters

In this method, you measure one pulse of a known width using your signal and derive the frequency of your signal from the result. This method is good for high frequency signals.

In this method, you route a pulse of known duration (T) to the Gate of a counter. You can generate the pulse using a second counter. You also can generate the pulse externally and connect it to a PFI or RTSI terminal. You only need to use one counter if you generate the pulse externally.

Route the signal to measure (F1) to the Source of the counter. Configure the counter for a single pulse-width measurement. If you measure the width of pulse T to be *N* periods of F1, the frequency of F1 is *N*/T.

Figure 7-12 illustrates this method. Another option would be to measure the width of a known period instead of a known pulse.

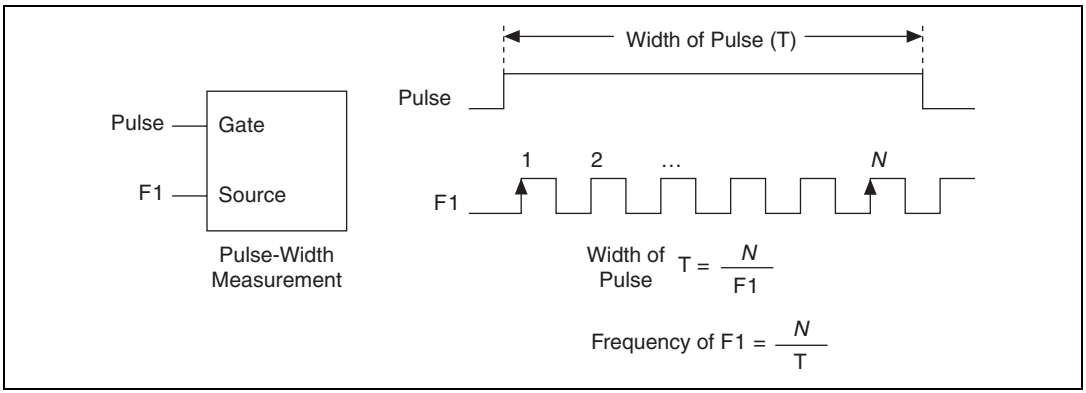


Figure 7-12. Method 2

Method 3—Measure Large Range of Frequencies Using Two Counters

By using two counters, you can accurately measure a signal that might be high or low frequency. This technique is called reciprocal frequency measurement. In this method, you generate a long pulse using the signal to measure. You then measure the long pulse with a known timebase. The M Series device can measure this long pulse more accurately than the faster input signal.

You can route the signal to measure to the Source input of Counter 0, as shown in Figure 7-13. Assume this signal to measure has frequency F1. Configure Counter 0 to generate a single pulse that is the width of *N* periods of the source input signal.

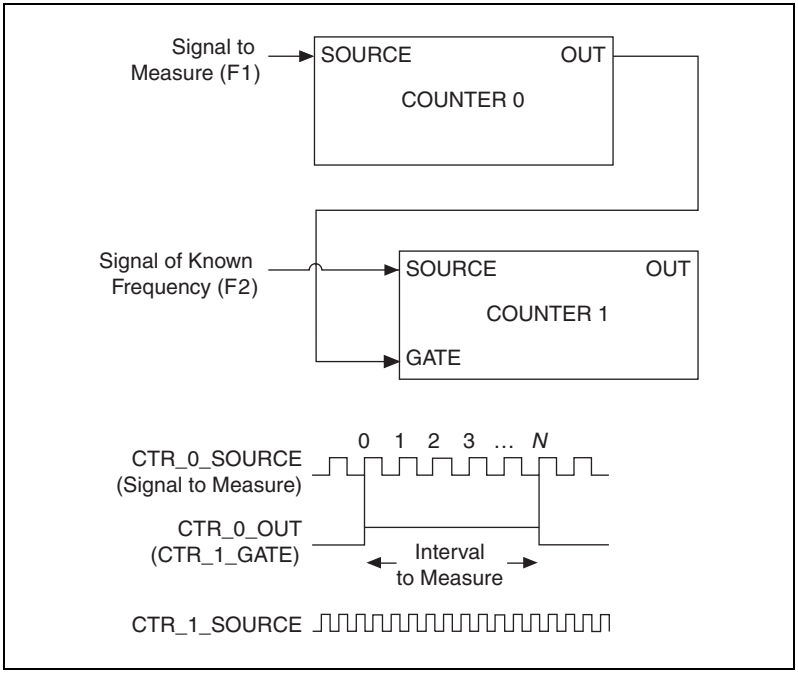


Figure 7-13. Method 3

Then route the Counter 0 Internal Output signal to the Gate input of Counter 1. You can route a signal of known frequency (F2) to the Counter 1 Source input. F2 can be 80MHzTimebase. For signals that might be slower than 0.02 Hz, use a slower known timebase. Configure Counter 1 to perform a single pulse-width measurement. Suppose the result is that the pulse width is J periods of the F2 clock.

From Counter 0, the length of the pulse is *N*/F1. From Counter 1, the length of the same pulse is J/F2. Therefore, the frequency of F1 is given by F1 = F2 * (*N*/J).

Choosing a Method for Measuring Frequency

The best method to measure frequency depends on several factors including the expected frequency of the signal to measure, the desired accuracy, how many counters are available, and how long the measurement can take.

- Method 1 uses only one counter. It is a good method for many applications. However, the accuracy of the measurement decreases as the frequency increases.

  Consider a frequency measurement on a 50 kHz signal using an 80 MHz Timebase. This frequency corresponds to 1600 cycles of the 80 MHz Timebase. Your measurement may return 1600 ± 1 cycles depending on the phase of the signal with respect to the timebase. As your frequency becomes larger, this error of ±1 cycle becomes more significant; Table 7-1 illustrates this point.

Table 7-1. Frequency Measurement Method 1

Task	Equation	Example 1	Example 2
Actual Frequency to Measure	F1	50 kHz	5 MHz
Timebase Frequency	Ft	80 MHz	80 MHz
Actual Number of Timebase Periods	Ft/F1	1600	16
Worst Case Measured Number of Timebase Periods	(Ft/F1) – 1	1599	15
Measured Frequency	Ft F1/(Ft – F1)	50.031 kHz	5.33 MHz
Error	[Ft F1/(Ft – F1)] – F1	31 Hz	333 kHz
Error %	[Ft/(Ft – F1)] – 1	0.06%	6.67%

- Method 1b (measuring K periods of F1) improves the accuracy of the measurement. A disadvantage of Method 1b is that you have to take K + 1 measurements. These measurements take more time and consume some of the available PCI or PXI bandwidth.
- Method 2 is accurate for high frequency signals. However, the accuracy decreases as the frequency of the signal to measure decreases. At very low frequencies, Method 2 may be too inaccurate

for your application. Another disadvantage of Method 2 is that it requires two counters (if you cannot provide an external signal of known width). An advantage of Method 2 is that the measurement completes in a known amount of time.

- Method 3 measures high and low frequency signals accurately. However, it requires two counters.

Table 7-2 summarizes some of the differences in methods of measuring frequency.

Table 7-2. Frequency Measurement Method Comparison

Method	Number of Counters Used	Number of Measurements Returned	Measures High Frequency Signals Accurately	Measures Low Frequency Signals Accurately
1	1	1	Poor	Good
1b	1	Many	Fair	Good
2	1 or 2	1	Good	Poor
3	2	1	Good	Good

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Position Measurement

You can use the counters to perform position measurements with quadrature encoders or two-pulse encoders. You can measure angular position with X1, X2, and X4 angular encoders. Linear position can be measured with two-pulse encoders. You can choose to do either a single point (on-demand) position measurement or a buffered (sample clock) position measurement. You must arm a counter to begin position measurements.

Measurements Using Quadrature Encoders

The counters can perform measurements of quadrature encoders that use X1, X2, or X4 encoding. A quadrature encoder can have up to three channels—channels A, B, and Z.

X1 Encoding

When channel A leads channel B in a quadrature cycle, the counter increments. When channel B leads channel A in a quadrature cycle, the counter decrements. The amount of increments and decrements per cycle depends on the type of encoding—X1, X2, or X4.

Figure 7-14 shows a quadrature cycle and the resulting increments and decrements for X1 encoding. When channel A leads channel B, the increment occurs on the rising edge of channel A. When channel B leads channel A, the decrement occurs on the falling edge of channel A.

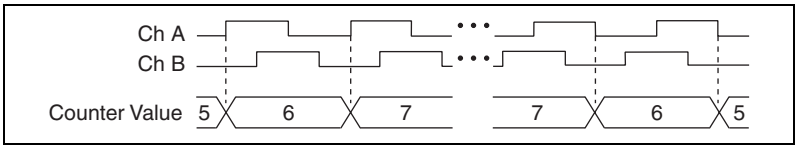


Figure 7-14. X1 Encoding

X2 Encoding

The same behavior holds for X2 encoding except the counter increments or decrements on each edge of channel A, depending on which channel leads the other. Each cycle results in two increments or decrements, as shown in Figure 7-15.

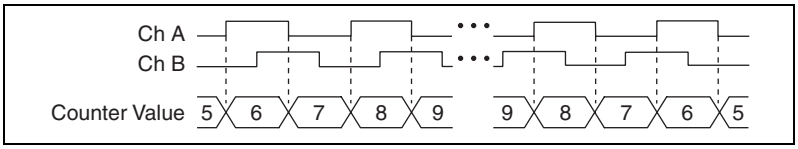


Figure 7-15. X2 Encoding

X4 Encoding

Similarly, the counter increments or decrements on each edge of channels A and B for X4 encoding. Whether the counter increments or decrements depends on which channel leads the other. Each cycle results in four increments or decrements, as shown in Figure 7-16.

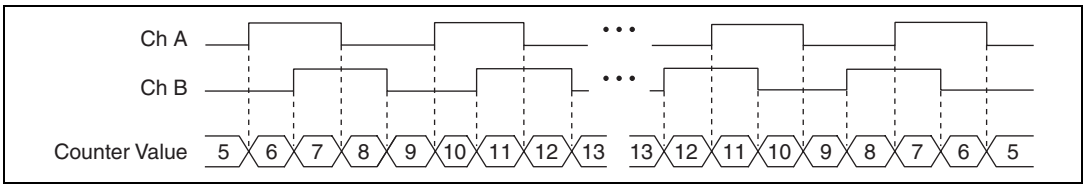


Figure 7-16. X4 Encoding

Channel Z Behavior

Some quadrature encoders have a third channel, channel Z, which is also referred to as the index channel. A high level on channel Z causes the counter to be reloaded with a specified value in a specified phase of the quadrature cycle. You can program this reload to occur in any one of the four phases in a quadrature cycle.

Channel Z behavior—when it goes high and how long it stays high—differs with quadrature encoder designs. You must refer to the documentation for your quadrature encoder to obtain timing of channel Z with respect to channels A and B. You must then ensure that channel Z is high during at least a portion of the phase you specify for reload. For instance, in Figure 7-17, channel Z is never high when channel A is high and channel B is low. Thus, the reload must occur in some other phase.

In Figure 7-17, the reload phase is when both channel A and channel B are low. The reload occurs when this phase is true and channel Z is high. Incrementing and decrementing takes priority over reloading. Thus, when the channel B goes low to enter the reload phase, the increment occurs first. The reload occurs within one maximum timebase period after the reload phase becomes true. After the reload occurs, the counter continues to count as before. The figure illustrates channel Z reload with X4 decoding.

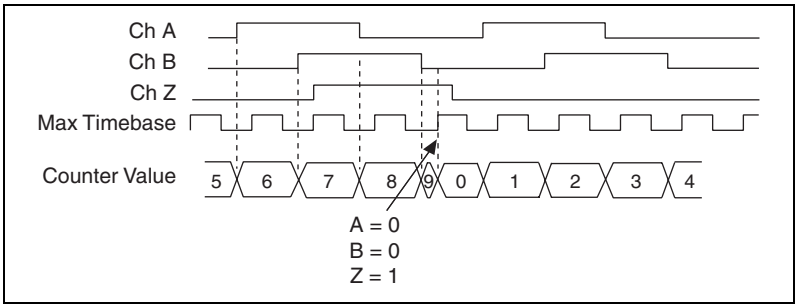


Figure 7-17. Channel Z Reload with X4 Decoding

Measurements Using Two Pulse Encoders

The counter supports two pulse encoders that have two channels—channels A and B.

The counter increments on each rising edge of channel A. The counter decrements on each rising edge of channel B, as shown in Figure 7-18.

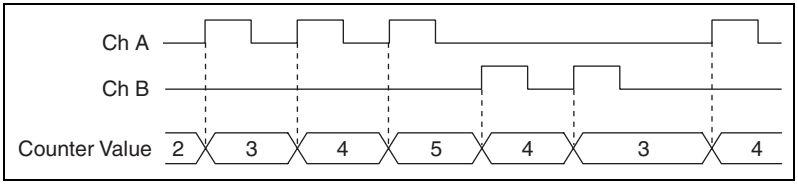


Figure 7-18. Measurements Using Two Pulse Encoders

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Two-Signal Edge-Separation Measurement

Two-signal edge-separation measurement is similar to pulse-width measurement, except that there are two measurement signals—Aux and Gate. An active edge on the Aux input starts the counting and an active edge on the Gate input stops the counting. You must arm a counter to begin a two edge separation measurement.

After the counter has been armed and an active edge occurs on the Aux input, the counter counts the number of rising (or falling) edges on the Source. The counter ignores additional edges on the Aux input.

The counter stops counting upon receiving an active edge on the Gate input. The counter stores the count in a hardware save register.

You can configure the rising or falling edge of the Aux input to be the active edge. You can configure the rising or falling edge of the Gate input to be the active edge.

Use this type of measurement to count events or measure the time that occurs between edges on two signals. This type of measurement is sometimes referred to as start/stop trigger measurement, second gate measurement, or A-to-B measurement.

Single Two-Signal Edge-Separation Measurement

With single two-signal edge-separation measurement, the counter counts the number of rising (or falling) edges on the Source input occurring between an active edge of the Gate signal and an active edge of the Aux signal. The counter then stores the count in a hardware save register and ignores other edges on its inputs. Software then reads the stored count.

Figure 7-19 shows an example of a single two-signal edge-separation measurement.

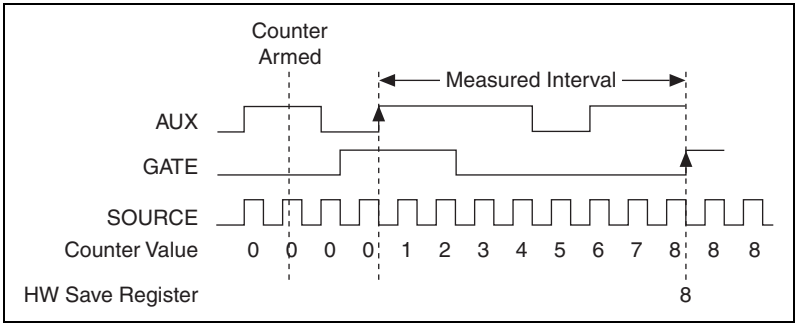


Figure 7-19. Single Two-Signal Edge-Separation Measurement

Buffered Two-Signal Edge-Separation Measurement

Buffered and single two-signal edge-separation measurements are similar, but buffered measurement measures multiple intervals.

The counter counts the number of rising (or falling) edges on the Source input occurring between an active edge of the Gate signal and an active edge of the Aux signal. The counter then stores the count in a hardware save register. On the next active edge of the Gate signal, the counter begins another measurement. A DMA controller transfers the stored values to host memory.

Figure 7-20 shows an example of a buffered two-signal edge-separation measurement.

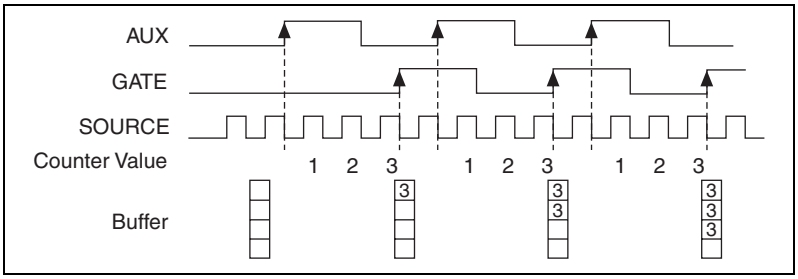


Figure 7-20. Buffered Two-Signal Edge-Separation Measurement

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Counter Output Applications

Simple Pulse Generation

Single Pulse Generation

The counter can output a single pulse. The pulse appears on the Counter *n* Internal Output signal of the counter.

You can specify a delay from when the counter is armed to the beginning of the pulse. The delay is measured in terms of a number of active edges of the Source input.

You can specify a pulse width. The pulse width is also measured in terms of a number of active edges of the Source input. You also can specify the active edge of the Source input (rising or falling).

Figure 7-21 shows a generation of a pulse with a pulse delay of four and a pulse width of three (using the rising edge of Source).

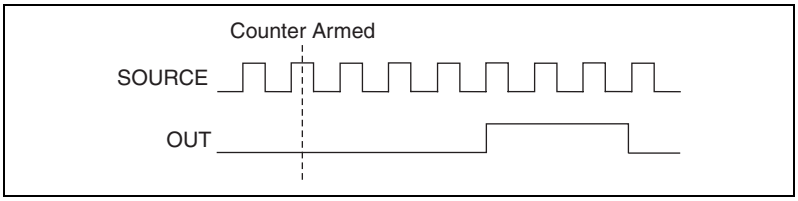


Figure 7-21. Single Pulse Generation

Single Pulse Generation with Start Trigger

The counter can output a single pulse in response to one pulse on a hardware Start Trigger signal. The pulse appears on the Counter *n* Internal Output signal of the counter.

You can route the Start Trigger signal to the Gate input of the counter. You can specify a delay from the Start Trigger to the beginning of the pulse. You also can specify the pulse width. The delay and pulse width are measured in terms of a number of active edges of the Source input.

After the Start Trigger signal pulses once, the counter ignores the Gate input.

Figure 7-22 shows a generation of a pulse with a pulse delay of four and a pulse width of three (using the rising edge of Source).

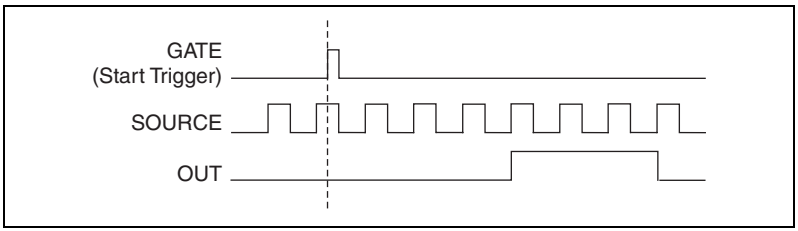


Figure 7-22. Single Pulse Generation with Start Trigger

Retriggerable Single Pulse Generation

The counter can output a single pulse in response to each pulse on a hardware Start Trigger signal. The pulses appear on the Counter *n* Internal Output signal of the counter.

You can route the Start Trigger signal to the Gate input of the counter. You can specify a delay from the Start Trigger to the beginning of each pulse. You also can specify the pulse width. The delay and pulse width are measured in terms of a number of active edges of the Source input.

The counter ignores the Gate input while a pulse generation is in progress. After the pulse generation is finished, the counter waits for another Start Trigger signal to begin another pulse generation.

Figure 7-23 shows a generation of two pulses with a pulse delay of five and a pulse width of three (using the rising edge of Source).

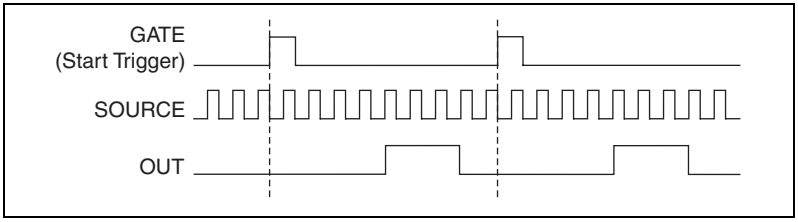


Figure 7-23. Retriggerable Single Pulse Generation

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Pulse Train Generation

Continuous Pulse Train Generation

This function generates a train of pulses with programmable frequency and duty cycle. The pulses appear on the Counter *n* Internal Output signal of the counter.

You can specify a delay from when the counter is armed to the beginning of the pulse train. The delay is measured in terms of a number of active edges of the Source input.

You specify the high and low pulse widths of the output signal. The pulse widths are also measured in terms of a number of active edges of the Source

input. You also can specify the active edge of the Source input (rising or falling).

The counter can begin the pulse train generation as soon as the counter is armed, or in response to a hardware Start Trigger. You can route the Start Trigger to the Gate input of the counter.

You also can use the Gate input of the counter as a Pause Trigger (if it is not used as a Start Trigger). The counter pauses pulse generation when the Pause Trigger is active.

Figure 7-24 shows a continuous pulse train generation (using the rising edge of Source).

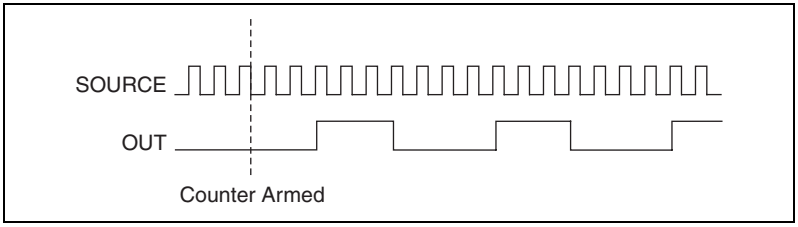


Figure 7-24. Continuous Pulse Train Generation

Continuous pulse train generation is sometimes called frequency division. If the high and low pulse widths of the output signal are *M* and *N* periods, then the frequency of the Counter *n* Internal Output signal is equal to the frequency of the Source input divided by *M* + *N*.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Frequency Generation

You can generate a frequency by using a counter in pulse train generation mode or by using the frequency generator circuit.

Using the Frequency Generator

The frequency generator can output a square wave at many different frequencies. The frequency generator is independent of the two general-purpose 32-bit counter/timer modules on M Series devices.

Figure 7-25 shows a block diagram of the frequency generator.

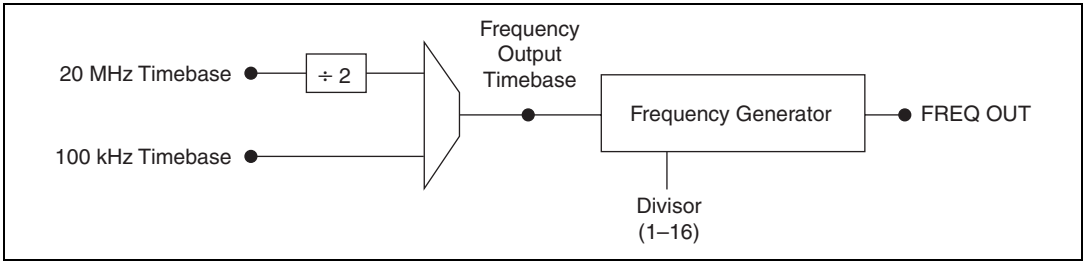


Figure 7-25. Frequency Generator Block Diagram

The frequency generator generates the Frequency Output signal. The Frequency Output signal is the Frequency Output Timebase divided by a number you select from 1 to 16. The Frequency Output Timebase can be either the 20 MHz Timebase divided by 2 or the 100 kHz Timebase.

The duty cycle of Frequency Output is 50% if the divider is either 1 or an even number. For an odd divider, suppose the divider is set to D. In this case, Frequency Output is low for (D + 1)/2 cycles and high for (D – 1)/2 cycles of the Frequency Output Timebase.

Figure 7-26 shows the output waveform of the frequency generator when the divider is set to 5.

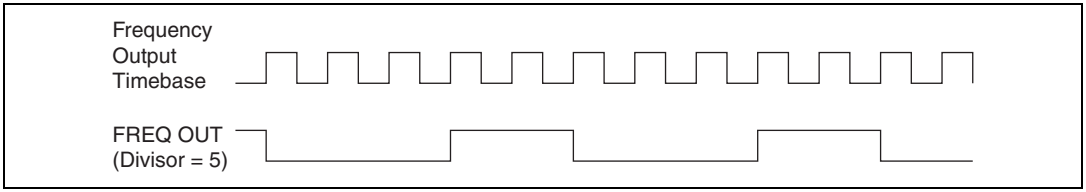


Figure 7-26. Frequency Generator Output Waveform

Frequency Output can be routed out to any PFI <0..15> or RTSI <0..7> terminal. All PFI terminals are set to high-impedance at startup. The FREQ OUT signal also can be routed to DO Sample Clock and DI Sample Clock.

In software, program the frequency generator as you would program one of the counters for pulse train generation.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Frequency Division

The counters can generate a signal with a frequency that is a fraction of an input signal. This function is equivalent to continuous pulse train generation.

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Pulse Generation for ETS

In the equivalent time sampling (ETS) application, the counter produces a pulse on the output a specified delay after an active edge on Gate. After each active edge on Gate, the counter cumulatively increments the delay between the Gate and the pulse on the output by a specified amount. Thus, the delay between the Gate and the pulse produced successively increases.

The increase in the delay value can be between 0 and 255. For instance, if you specify the increment to be 10, the delay between the active Gate edge and the pulse on the output will increase by 10 every time a new pulse is generated.

Suppose you program your counter to generate pulses with a delay of 100 and pulse width of 200 each time it receives a trigger. Furthermore, suppose you specify the delay increment to be 10. On the first trigger, your pulse delay will be 100, on the second it will be 110, on the third it will be 120; the process will repeat in this manner until the counter is disarmed. The counter ignores any Gate edge that is received while the pulse triggered by the previous Gate edge is in progress.

The waveform thus produced at the counter's output can be used to provide timing for undersampling applications where a digitizing system can sample repetitive waveforms that are higher in frequency than the Nyquist frequency of the system. Figure 7-27 shows an example of pulse generation for ETS; the delay from the trigger to the pulse increases after each subsequent Gate active edge.

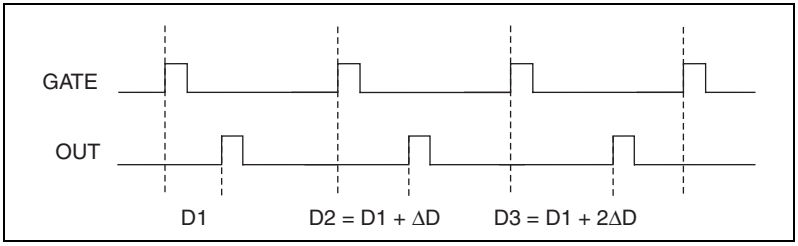


Figure 7-27. Pulse Generation for ETS

For information about connecting counter signals, refer to the *Default Counter/Timer Pinouts* section.

Counter Timing Signals

M Series devices feature the following counter timing signals.

- Counter *n* Source
- Counter *n* Gate
- Counter *n* Aux
- Counter *n* A
- Counter *n* B
- Counter *n* Z
- Counter *n* Up_Down
- Counter *n* HW Arm
- Counter *n* Internal Output
- Counter *n* TC
- Frequency Output

In this section, *n* refers to either Counter 0 or 1. For example, Counter *n* Source refers to two signals—Counter 0 Source (the source input to Counter 0) and Counter 1 Source (the source input to Counter 1).

Counter *n* Source Signal

The selected edge of the Counter *n* Source signal increments and decrements the counter value depending on the application the counter is performing. Table 7-3 lists how this terminal is used in various applications.

Table 7-3. Counter Applications and Counter *n* Source

Application	Purpose of Source Terminal
Pulse Generation	Counter Timebase
One Counter Time Measurements	Counter Timebase
Two Counter Time Measurements	Input Terminal
Non-Buffered Edge Counting	Input Terminal
Buffered Edge Counting	Input Terminal
Two-Edge Separation	Counter Timebase

Routing a Signal to Counter *n* Source

Each counter has independent input selectors for the Counter *n* Source signal. Any of the following signals can be routed to the Counter *n* Source input.

- 80 MHz Timebase
- 20 MHz Timebase
- 100 kHz Timebase
- RTSI <0..7>
- PFI <0..15>
- PXI_CLK10
- PXI_STAR
- Analog Comparison Event

In addition, Counter 1 TC or Counter 1 Gate can be routed to Counter 0 Source. Counter 0 TC or Counter 0 Gate can be routed to Counter 1 Source.

Some of these options may not be available in some driver software.

Routing Counter *n* Source to an Output Terminal

You can route Counter *n* Source out to any PFI <0..15> or RTSI <0..7> terminal. All PFIs are set to high-impedance at startup.

Counter *n* Gate Signal

The Counter *n* Gate signal can perform many different operations depending on the application including starting and stopping the counter, and saving the counter contents.

Routing a Signal to Counter *n* Gate

Each counter has independent input selectors for the Counter *n* Gate signal. Any of the following signals can be routed to the Counter *n* Gate input.

- RTSI <0..7>
- PFI <0..15>
- ai/ReferenceTrigger
- ai/StartTrigger
- ai/SampleClock
- ai/ConvertClock
- ao/SampleClock
- di/SampleClock
- do/SampleClock
- PXI_STAR
- Change Detection Event
- Analog Comparison Event

In addition, Counter 1 Internal Output or Counter 1 Source can be routed to Counter 0 Gate. Counter 0 Internal Output or Counter 0 Source can be routed to Counter 1 Gate.

Some of these options may not be available in some driver software.

Routing Counter *n* Gate to an Output Terminal

You can route Counter *n* Gate out to any PFI <0..15> or RTSI <0..7> terminal. All PFIs are set to high-impedance at startup.

Counter *n* Aux Signal

The Counter *n* Aux signal indicates the first edge in a two-signal edge-separation measurement.

Routing a Signal to Counter *n* Aux

Each counter has independent input selectors for the Counter *n* Aux signal. Any of the following signals can be routed to the Counter *n* Aux input.

- RTSI <0..7>
- PFI <0..15>
- ai/ReferenceTrigger
- ai/StartTrigger
- PXI_STAR
- Analog Comparison Event

In addition, Counter 1 Internal Output, Counter 1 Gate, Counter 1 Source, or Counter 0 Gate can be routed to Counter 0 Aux. Counter 0 Internal Output, Counter 0 Gate, Counter 0 Source, or Counter 1 Gate can be routed to Counter 1 Aux.

Some of these options may not be available in some driver software.

Counter *n* A, Counter *n* B, and Counter *n* Z Signals

Counter *n* B can control the direction of counting in edge counting applications. Use the A, B, and Z inputs to each counter when measuring quadrature encoders or measuring two pulse encoders.

Routing Signals to A, B, and Z Counter Inputs

Each counter has independent input selectors for each of the A, B, and Z inputs. Any of the following signals can be routed to each input.

- RTSI <0..7>
- PFI <0..15>
- PXI_STAR
- Analog Comparison Event

Routing Counter *n* Z Signal to an Output Terminal

You can route Counter *n* Z out to RTSI <0..7>.

Counter *n* Up_Down Signal

Counter *n* Up_Down is another name for the Counter *n* B signal.

Counter *n* HW Arm Signal

The Counter *n* HW Arm signal enables a counter to begin an input or output function.

To begin any counter input or output function, you must first enable, or arm, the counter. In some applications, such as buffered semi-period measurement, the counter begins counting when it is armed. In other applications, such as single pulse-width measurement, the counter begins waiting for the Gate signal when it is armed. Counter output operations can use the arm signal in addition to a start trigger.

Software can arm a counter or configure counters to be armed on a hardware signal. Software calls this hardware signal the Arm Start Trigger. Internally, software routes the Arm Start Trigger to the Counter *n* HW Arm input of the counter.

Routing Signals to Counter *n* HW Arm Input

Any of the following signals can be routed to the Counter *n* HW Arm input.

- RTSI <0..7>
- PFI <0..15>
- ai/ReferenceTrigger
- ai/StartTrigger
- PXI_STAR
- Analog Comparison Event

Counter 1 Internal Output can be routed to Counter 0 HW Arm. Counter 0 Internal Output can be routed to Counter 1 HW Arm.

Some of these options may not be available in some driver software.

Counter *n* Internal Output and Counter *n* TC Signals

The Counter *n* Internal Output signal changes in response to Counter *n* TC.

The two software-selectable output options are pulse output on TC and toggle output on TC. The output polarity is software-selectable for both options.

With pulse or pulse train generation tasks, the counter drives the pulse(s) on the Counter *n* Internal Output signal. The Counter *n* Internal Output signal can be internally routed to be a counter/timer input or an "external" source for AI, AO, DI, or DO timing signals.

Routing Counter *n* Internal Output to an Output Terminal

You can route Counter *n* Internal Output to any PFI <0..15> or RTSI <0..7> terminal. All PFIs are set to high-impedance at startup.

Frequency Output Signal

The Frequency Output (FREQ OUT) signal is the output of the frequency output generator.

Routing Frequency Output to a Terminal

You can route Frequency Output to any PFI <0..15> terminal. All PFIs are set to high-impedance at startup. The FREQ OUT signal also can be routed to DO Sample Clock and DI Sample Clock.

Default Counter/Timer Pinouts

By default, NI-DAQmx routes the counter/timer inputs and outputs to the PFI pins, shown in Table 7-4. To find the default NI-DAQmx counter/timer pins for the PCI-6221 (37-pin), USB-62*xx* Screw Terminal, and USB-62*xx* BNC devices, refer to Appendix A, *Device-Specific Information*.

Table 7-4. 68-Pin Device Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)

Table 7-4. 68-Pin Device Default NI-DAQmx Counter/Timer Pins (Continued)

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

You can use these defaults or select other sources and destinations for the counter/timer signals in NI-DAQmx. Refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information about how to connect your signals for common counter measurements and generations. M Series default PFI lines for counter functions are listed in *Physical Channels* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Counter Triggering

Counters support three different triggering actions—arm start, start, and pause.

Arm Start Trigger

To begin any counter input or output function, you must first enable, or arm, the counter. Software can arm a counter or configure counters to be armed on a hardware signal. Software calls this hardware signal the Arm Start Trigger. Internally, software routes the Arm Start Trigger to the Counter *n* HW Arm input of the counter.

For counter output operations, you can use it in addition to the start and pause triggers. For counter input operations, you can use the arm start trigger to have start trigger-like behavior. The arm start trigger can be used for synchronizing multiple counter input and output tasks.

When using an arm start trigger, the arm start trigger source is routed to the Counter *n* HW Arm signal.

Start Trigger

For counter output operations, a start trigger can be configured to begin a finite or continuous pulse generation. Once a continuous generation has triggered, the pulses continue to generate until you stop the operation in software. For finite generations, the specified number of pulses is generated and the generation stops unless you use the retriggerable attribute. When you use this attribute, subsequent start triggers cause the generation to restart.

When using a start trigger, the start trigger source is routed to the Counter *n* Gate signal input of the counter.

Counter input operations can use the arm start trigger to have start trigger-like behavior.

Pause Trigger

You can use pause triggers in edge counting and continuous pulse generation applications. For edge counting acquisitions, the counter stops counting edges while the external trigger signal is low and resumes when the signal goes high or vice versa. For continuous pulse generations, the counter stops generating pulses while the external trigger signal is low and resumes when the signal goes high or vice versa.

When using a pause trigger, the pause trigger source is routed to the Counter *n* Gate signal input of the counter.

Other Counter Features

Cascading Counters

You can internally route the Counter *n* Internal Output and Counter *n* TC signals of each counter to the Gate inputs of the other counter. By cascading two counters together, you can effectively create a 64-bit counter. By cascading counters, you also can enable other applications. For example, to improve the accuracy of frequency measurements, use reciprocal frequency measurement, as described in the *Method 3—Measure Large Range of Frequencies Using Two Counters* section.

Counter Filters

You can enable a programmable debouncing filter on each PFI, RTSI, or PXI_STAR signal. When the filters are enabled, your device samples the input on each rising edge of a filter clock. M Series devices use an onboard oscillator to generate the filter clock with a 40 MHz frequency.

Note NI-DAQmx *only* supports filters on counter inputs.

The following is an example of low to high transitions of the input signal. High to low transitions work similarly.

Assume that an input terminal has been low for a long time. The input terminal then changes from low to high, but glitches several times. When the filter clock has sampled the signal high on N consecutive edges, the low to high transition is propagated to the rest of the circuit. The value of N depends on the filter setting; refer to Table 7-5.

Table 7-5. Filters

Filter Setting	N (Filter Clocks Needed to Pass Signal)	Pulse Width Guaranteed to Pass Filter	Pulse Width Guaranteed to Not Pass Filter
125 ns	5	125 ns	100 ns
6.425 µs	257	6.425 µs	6.400 µs
2.56 ms	~101,800	2.56 ms	2.54 ms
Disabled	—	—	—

The filter setting for each input can be configured independently. On power up, the filters are disabled. Figure 7-28 shows an example of a low to high transition on an input that has its filter set to 125 ns (N = 5).

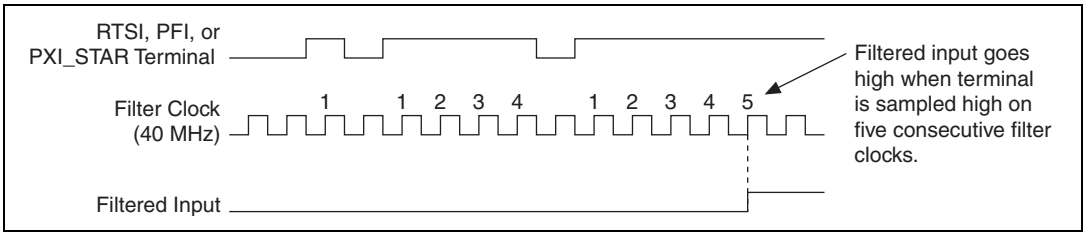


Figure 7-28. Filter Example

Enabling filters introduces jitter on the input signal. For the 125 ns and 6.425 µs filter settings, the jitter is up to 25 ns. On the 2.56 ms setting, the jitter is up to 10.025 µs.

When a PFI input is routed directly to RTSI, or a RTSI input is routed directly to PFI, the M Series device does not use the filtered version of the input signal.

Refer to the KnowledgeBase document, *Digital Filtering with M Series*, for more information about digital filters and counters. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rddfms`.

Prescaling

Prescaling allows the counter to count a signal that is faster than the maximum timebase of the counter. M Series devices offer 8X and 2X prescaling on each counter (prescaling can be disabled). Each prescaler consists of a small, simple counter that counts to eight (or two) and rolls over. This counter can run faster than the larger counters, which simply count the rollovers of this smaller counter. Thus, the prescaler acts as a frequency divider on the Source and puts out a frequency that is one-eighth (or one-half) of what it is accepting.

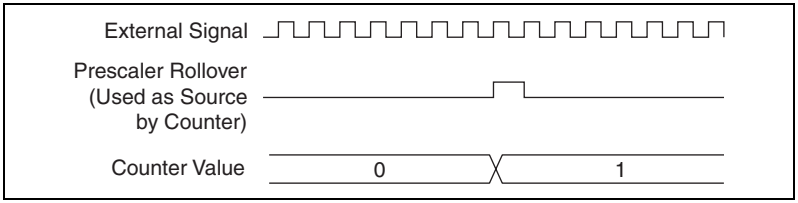


Figure 7-29. Prescaling

Prescaling is intended to be used for frequency measurement where the measurement is made on a continuous, repetitive signal. The prescaling counter cannot be read; therefore, you cannot determine how many edges have occurred since the previous rollover. Prescaling can be used for event counting provided it is acceptable to have an error of up to seven (or one). Prescaling can be used when the counter Source is an external signal. Prescaling is not available if the counter Source is one of the internal timebases (80MHzTimebase, 20MHzTimebase, or 100kHzTimebase).

Duplicate Count Prevention

Duplicate count prevention (or synchronous counting mode) ensures that a counter returns correct data in applications that use a slow or non-periodic external source. Duplicate count prevention applies only to buffered counter applications such as measuring frequency or period. In such buffered applications, the counter should store the number of times an external Source pulses between rising edges on the Gate signal.

Example Application That Works Correctly (No Duplicate Counting)

Figure 7-30 shows an external buffered signal as the period measurement Source.

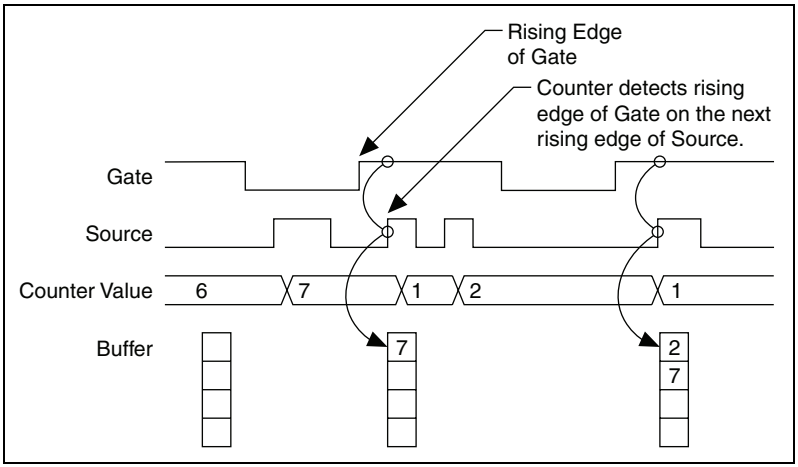


Figure 7-30. Duplicate Count Prevention Example

On the first rising edge of the Gate, the current count of 7 is stored. On the next rising edge of the Gate, the counter stores a 2 since two Source pulses occurred after the previous rising edge of Gate.

The counter synchronizes or samples the Gate signal with the Source signal, so the counter does not detect a rising edge in the Gate until the next Source pulse. In this example, the counter stores the values in the buffer on the first rising Source edge after the rising edge of Gate. The details of when exactly the counter synchronizes the Gate signal vary depending on the synchronization mode. Synchronization modes are described in the *Synchronization Modes* section.

Example Application That Works Incorrectly (Duplicate Counting)

In Figure 7-31, after the first rising edge of Gate, no Source pulses occur, so the counter does not write the correct data to the buffer.

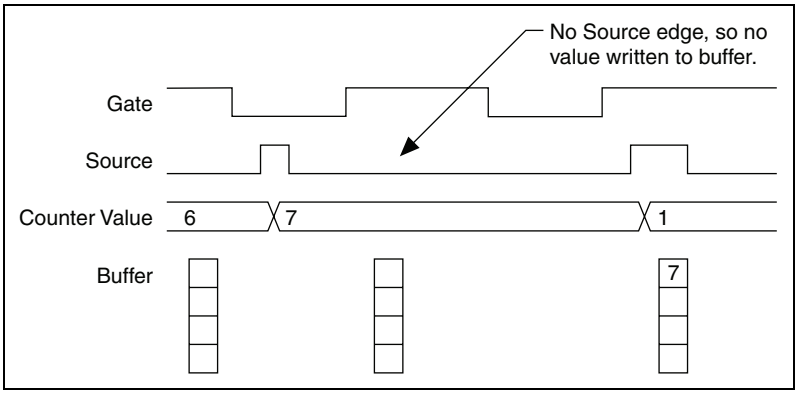


Figure 7-31. Duplicate Count Example

Example Application That Prevents Duplicate Count

With duplicate count prevention enabled, the counter synchronizes both the Source and Gate signals to the 80 MHz Timebase. By synchronizing to the timebase, the counter detects edges on the Gate even if the Source does not pulse. This enables the correct current count to be stored in the buffer even if no Source edges occur between Gate signals, as shown in Figure 7-32.

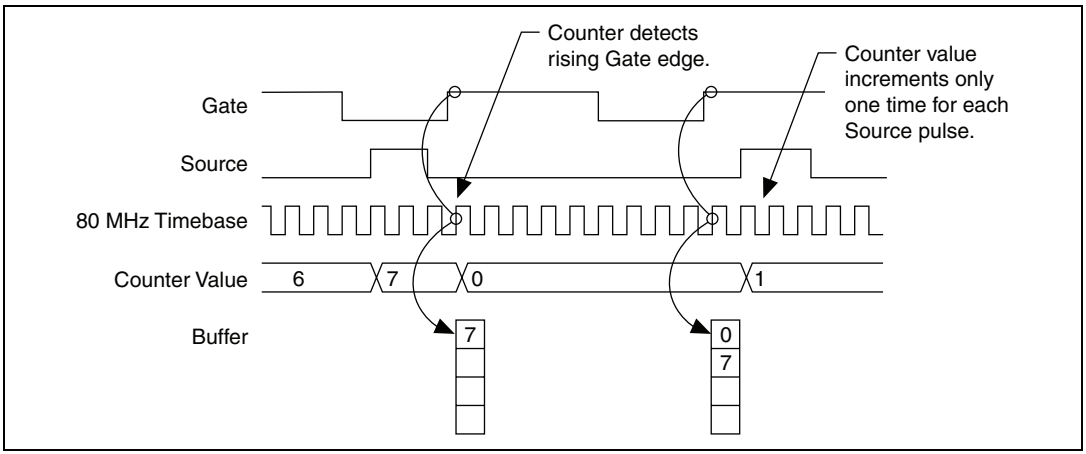


Figure 7-32. Duplicate Count Prevention Example

Even if the Source pulses are long, the counter increments only once for each Source pulse.

Normally, the counter value and Counter *n* Internal Output signals change synchronously to the Source signal. With duplicate count prevention, the counter value and Counter *n* Internal Output signals change synchronously to the 80 MHz Timebase.

Note that duplicate count prevention should only be used if the frequency of the Source signal is 20 MHz or less.

When To Use Duplicate Count Prevention

You should use duplicate count prevention if the following conditions are true:

- You are making a counter measurement.
- You are using an external signal (such as PFI *x*) as the counter Source.
- The frequency of the external source is 20 MHz or less.
- You can have the counter value and output to change synchronously with the 80 MHz Timebase.

In all other cases, you should *not* use duplicate count prevention.

Enabling Duplicate Count Prevention in NI-DAQmx

You can enable duplicate count prevention in NI-DAQmx by setting the **Enable Duplicate Count Prevention** attribute/property. For specific information about finding the **Enable Duplicate Count Prevention** attribute/property, refer to the help file for the API you are using.

Synchronization Modes

The 32-bit counter counts up or down synchronously with the Source signal. The Gate signal and other counter inputs are asynchronous to the Source signal. So M Series devices synchronize these signals before presenting them to the internal counter.

M Series devices use one of three synchronization methods:

- 80 MHz source mode
- Other internal source mode
- External source mode

In DAQmx, the device uses 80 MHz source mode if you perform the following:

- Perform a position measurement
- Select duplicate count prevention

Otherwise, the mode depends on the signal that drives Counter *n* Source. Table 7-6 describes the conditions for each mode.

Table 7-6. Synchronization Mode Conditions

Duplicate Count Prevention Enabled	Type of Measurement	Signal Driving Counter *n* Source	Synchronization Mode
Yes	Any	Any	80 MHz Source
No	Position Measurement	Any	80 MHz Source
No	Any	80 MHz Timebase	80 MHz Source
No	All Except Position Measurement	20 MHz Timebase, 100 kHz Timebase, or PXI_CLK10	Other Internal Source
No	All Except Position Measurement	Any Other Signal (such as PFI or RTSI)	External Source

80 MHz Source Mode

In 80 MHz source mode, the device synchronizes signals on the rising edge of the source, and counts on the following rising edge of the source, as shown in Figure 7-33.

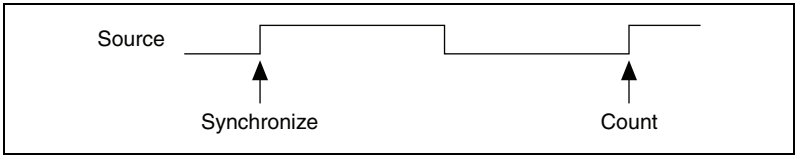


Figure 7-33. 80 MHz Source Mode

Other Internal Source Mode

In other internal source mode, the device synchronizes signals on the falling edge of the source, and counts on the following rising edge of the source, as shown in Figure 7-34.

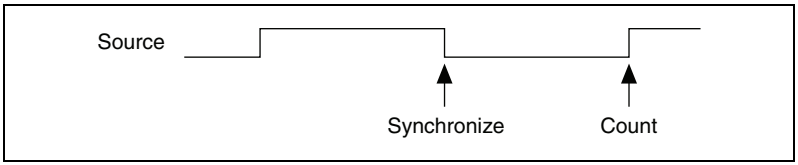


Figure 7-34. Other Internal Source Mode

External Source Mode

In external source mode, the device generates a delayed Source signal by delaying the Source signal by several nanoseconds. The device synchronizes signals on the rising edge of the delayed Source signal, and counts on the following rising edge of the source, as shown in Figure 7-35.

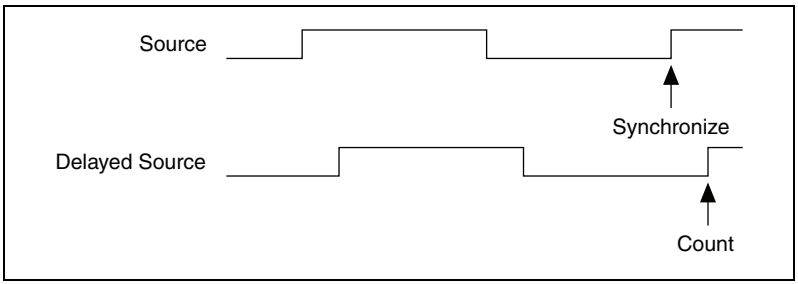


Figure 7-35. External Source Mode

8

PFI

M Series devices have up to 16 Programmable Function Interface (PFI) signals. In addition, M Series devices have up to 32 lines of bidirectional DIO signals.

Each PFI can be individually configured as the following.

- A static digital input
- A static digital output
- A timing input signal for AI, AO, DI, DO, or counter/timer functions
- A timing output signal from AI, AO, DI, DO, or counter/timer functions

Each PFI input also has a programmable debouncing filter. Figure 8-1 shows the circuitry of one PFI line. Each PFI line is similar.

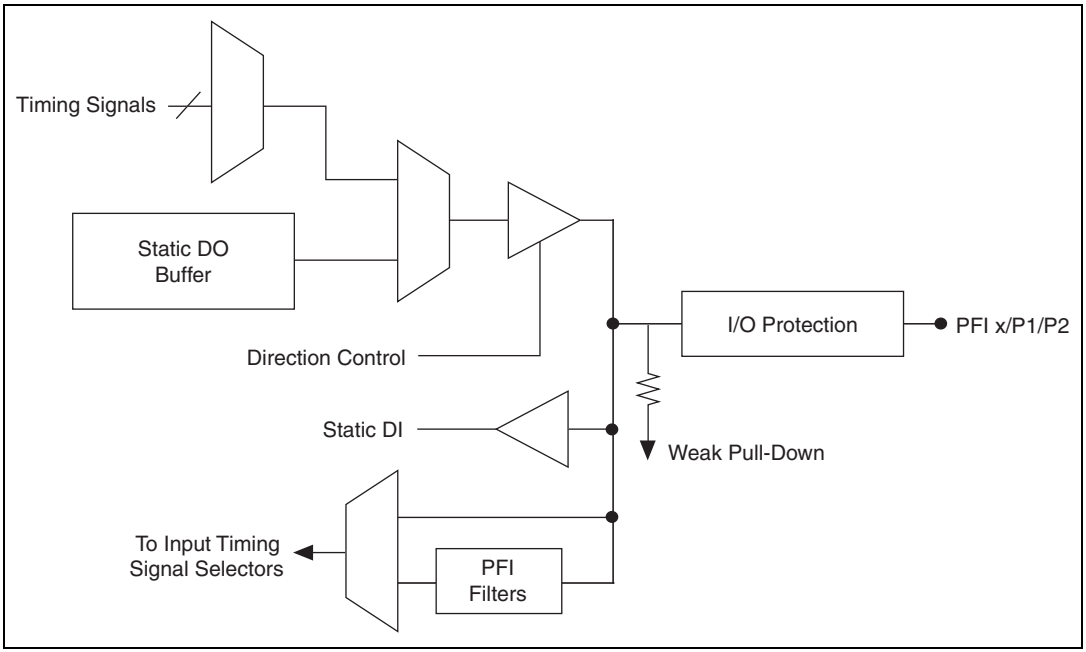


Figure 8-1. M Series PFI Circuitry

When a terminal is used as a timing input or output signal, it is called PFI *x* (where *x* is an integer from 0 to 15). When a terminal is used as a static digital input or output, it is called P1.*x* or P2.*x*. On the I/O connector, each terminal is labeled PFI *x*/P1 or PFI *x*/P2.

The voltage input and output levels and the current drive levels of the PFI signals are listed in the specifications of your device.

Using PFI Terminals as Timing Input Signals

Use PFI terminals to route external timing signals to many different M Series functions. Each PFI terminal can be routed to any of the following signals.

- AI Convert Clock
- AI Sample Clock
- AI Start Trigger
- AI Reference Trigger
- AI Pause Trigger
- AI Sample Clock Timebase
- AO Start Trigger
- AO Sample Clock
- AO Sample Clock Timebase
- AO Pause Trigger
- Counter input signals for either counter—Source, Gate, Aux, HW_Arm, A, B, Z
- DI Sample Clock
- DO Sample Clock

Most functions allow you to configure the polarity of PFI inputs and whether the input is edge or level sensitive.

Exporting Timing Output Signals Using PFI Terminals

You can route any of the following timing signals to any PFI terminal configured as an output.

- AI Convert Clock*
- AI Hold Complete Event
- AI Reference Trigger
- AI Sample Clock
- AI Start Trigger
- AO Sample Clock*
- AO Start Trigger
- Counter *n* Source
- Counter *n* Gate
- Counter *n* Internal Output
- Frequency Output
- PXI_STAR
- RTSI <0..7>
- Analog Comparison Event
- Change Detection Event
- DI Sample Clock*
- DO Sample Clock*

Note Signals with a * are inverted before being driven to a terminal; that is, these signals are active low.

Using PFI Terminals as Static Digital I/Os

Each PFI can be individually configured as a static digital input or a static digital output. When a terminal is used as a static digital input or output, it is called P1.*x* or P2.*x*. On the I/O connector, each terminal is labeled PFI *x*/P1.*x* or PFI *x*/P2.*x*.

In addition, M Series devices have up to 32 lines of bidirectional DIO signals.

Connecting PFI Input Signals

All PFI input connections are referenced to D GND. Figure 8-2 shows this reference, and how to connect an external PFI 0 source and an external PFI 2 source to two PFI terminals.

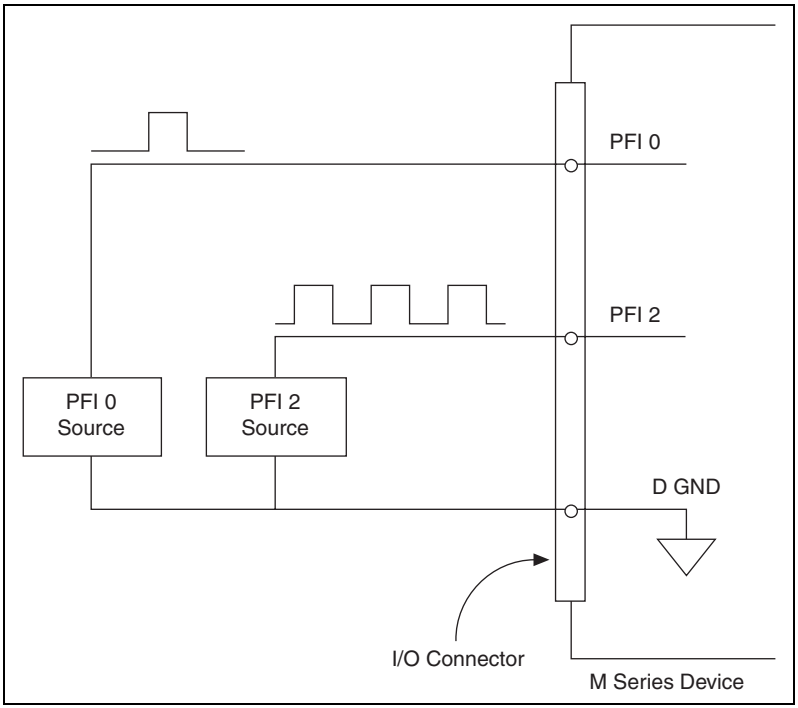


Figure 8-2. PFI Input Signals Connections

PFI Filters

You can enable a programmable debouncing filter on each PFI, RTSI, or PXI_STAR signal. When the filters are enabled, your device samples the input on each rising edge of a filter clock. M Series devices use an onboard oscillator to generate the filter clock with a 40 MHz frequency.

Note NI-DAQmx *only* supports filters on counter inputs.

The following is an example of low to high transitions of the input signal. High to low transitions work similarly.

Assume that an input terminal has been low for a long time. The input terminal then changes from low to high, but glitches several times. When the filter clock has sampled the signal high on N consecutive edges, the low to high transition is propagated to the rest of the circuit. The value of N depends on the filter setting; refer to Table 8-1.

Table 8-1. Filters

Filter Setting	N (Filter Clocks Needed to Pass Signal)	Pulse Width Guaranteed to Pass Filter	Pulse Width Guaranteed to Not Pass Filter
125 ns	5	125 ns	100 ns
6.425 µs	257	6.425 µs	6.400 µs
2.56 ms	~101,800	2.56 ms	2.54 ms
Disabled	—	—	—

The filter setting for each input can be configured independently. On power up, the filters are disabled. Figure 8-3 shows an example of a low to high transition on an input that has its filter set to 125 ns (N = 5).

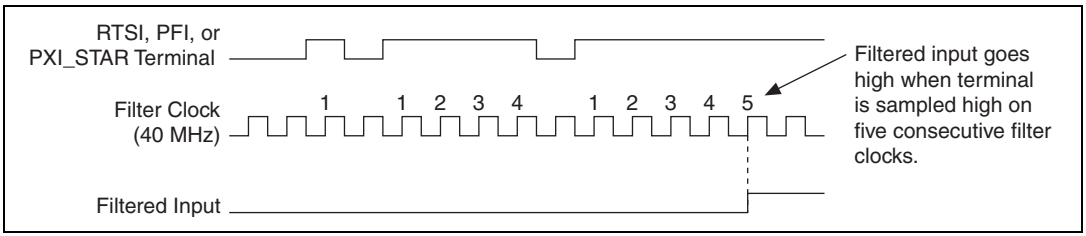


Figure 8-3. Filter Example

Enabling filters introduces jitter on the input signal. For the 125 ns and 6.425 µs filter settings, the jitter is up to 25 ns. On the 2.56 ms setting, the jitter is up to 10.025 µs.

When a PFI input is routed directly to RTSI, or a RTSI input is routed directly to PFI, the M Series device does not use the filtered version of the input signal.

Refer to the KnowledgeBase document, *Digital Filtering with M Series*, for more information about digital filters and counters. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rddfms`.

I/O Protection

Each DIO and PFI signal is protected against overvoltage, undervoltage, and overcurrent conditions as well as ESD events. However, you should avoid these fault conditions by following these guidelines.

- If you configure a PFI or DIO line as an output, do *not* connect it to any external signal source, ground, or power supply.
- If you configure a PFI or DIO line as an output, understand the current requirements of the load connected to these signals. Do *not* exceed the specified current output limits of the DAQ device. NI has several signal conditioning solutions for digital applications requiring high current drive.
- If you configure a PFI or DIO line as an input, do *not* drive the line with voltages outside of its normal operating range. The PFI or DIO lines have a smaller operating range than the AI signals.
- Treat the DAQ device as you would treat any static sensitive device. *Always* properly ground yourself and the equipment when handling the DAQ device or connecting to it.

Programmable Power-Up States

At system startup and reset, the hardware sets all PFI and DIO lines to high-impedance inputs by default. The DAQ device does not drive the signal high or low. Each line has a weak pull-down resistor connected to it, as described in the specifications document for your device.

NI-DAQmx 7.4 and later supports programmable power-up states for PFI and DIO lines. Software can program any value at power up to the P0, P1, or P2 lines. The PFI and DIO lines can be set as:

- A high-impedance input with a weak pull-down resistor (default)
- An output driving a 0
- An output driving a 1

Refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later for more information about setting power-up states in NI-DAQmx or MAX.

Note When using your M Series device to control an SCXI chassis, DIO lines 0, 1, 2, and 4 are used as communication lines and must be left to power-up in the default high-impedance state to avoid potential damage to these signals.

9

Digital Routing and Clock Generation

The digital routing circuitry has the following main functions.

- Manages the flow of data between the bus interface and the acquisition/generation sub-systems (analog input, analog output, digital I/O, and the counters). The digital routing circuitry uses FIFOs (if present) in each sub-system to ensure efficient data movement.
- Routes timing and control signals. The acquisition/generation sub-systems use these signals to manage acquisitions and generations. These signals can come from the following sources.
  - Your M Series device
  - Other devices in your system through RTSI
  - User input through the PFI terminals
  - User input through the PXI_STAR terminal
- Routes and generates the main clock signals for the M Series device.

Clock Routing

Figure 9-1 shows the clock routing circuitry of an M Series device.

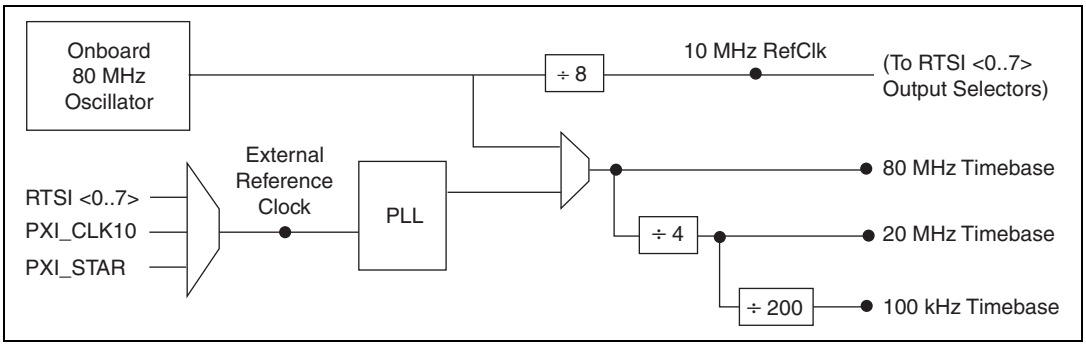


Figure 9-1. M Series Clock Routing Circuitry

80 MHz Timebase

The 80 MHz Timebase can be used as the Source input to the 32-bit general-purpose counter/timers.

The 80 MHz Timebase is generated from the following sources.

- Onboard oscillator
- External signal (by using the external reference clock)

20 MHz Timebase

The 20 MHz Timebase normally generates many of the AI and AO timing signals. The 20 MHz Timebase also can be used as the Source input to the 32-bit general-purpose counter/timers.

The 20 MHz Timebase is generated by dividing down the 80 MHz Timebase.

100 kHz Timebase

The 100 kHz Timebase can be used to generate many of the AI and AO timing signals. The 100 kHz Timebase also can be used as the Source input to the 32-bit general-purpose counter/timers.

The 100 kHz Timebase is generated by dividing down the 20 MHz Timebase by 200.

External Reference Clock

The external reference clock can be used as a source for the internal timebases (80 MHz Timebase, 20 MHz Timebase, and 100 kHz Timebase) on an M Series device. By using the external reference clock, you can synchronize the internal timebases to an external clock.

The following signals can be routed to drive the external reference clock.

- RTSI <0..7>
- PXI_CLK10
- PXI_STAR

The external reference clock is an input to a Phase-Lock Loop (PLL). The PLL generates the internal timebases.

10 MHz Reference Clock

The 10 MHz reference clock can be used to synchronize other devices to your M Series device. The 10 MHz reference clock can be routed to the RTSI <0..7> terminals. Other devices connected to the RTSI bus can use this signal as a clock input.

The 10 MHz reference clock is generated by dividing down the onboard oscillator.

Synchronizing Multiple Devices

With the RTSI bus and the routing capabilities of M Series devices, there are several ways to synchronize multiple devices depending on your application.

Note RTSI is *not* supported on USB devices.

To synchronize multiple devices to a common timebase, choose one device—the initiator—to generate the timebase. The initiator device routes its 10 MHz reference clock to one of the RTSI <0..7> signals.

All devices (including the initiator device) receive the 10 MHz reference clock from RTSI. This signal becomes the external reference clock. A PLL on each device generates the internal timebases synchronous to the external reference clock.

On PXI systems, you also can synchronize devices to PXI_CLK10. In this application the PXI chassis acts as the initiator. Each PXI module routes PXI_CLK10 to its external reference clock.

Another option in PXI systems is to use PXI_STAR. The Star Trigger controller device acts as the initiator and drives PXI_STAR with a clock signal. Each target device routes PXI_STAR to its external reference clock.

Once all of the devices are using or referencing a common timebase, you can synchronize operations across them by sending a common start trigger out across the RTSI bus and setting their sample clock rates to the same value.

Real-Time System Integration (RTSI)

Real-Time System Integration (RTSI) is a set of bused signals among devices that allows you to do the following:

- Use a common clock (or timebase) to drive the timing engine on multiple devices
- Share trigger signals between devices

Many National Instruments DAQ, motion, vision, and CAN devices support RTSI.

Note RTSI is *not* supported on USB devices.

In a PCI/PCI Express system, the RTSI bus consists of the RTSI bus interface and a ribbon cable. The bus can route timing and trigger signals between several functions on as many as five DAQ, vision, motion, or CAN devices in the computer.

In a PXI/PXI Express system, the RTSI bus consists of the RTSI bus interface and the PXI trigger signals on the PXI backplane. This bus can route timing and trigger signals between several functions on as many as seven DAQ devices in the system.

RTSI Connector Pinout

(PCI/PCI Express Devices) Figure 9-2 shows the RTSI connector pinout and Table 9-1 describes the RTSI signals.

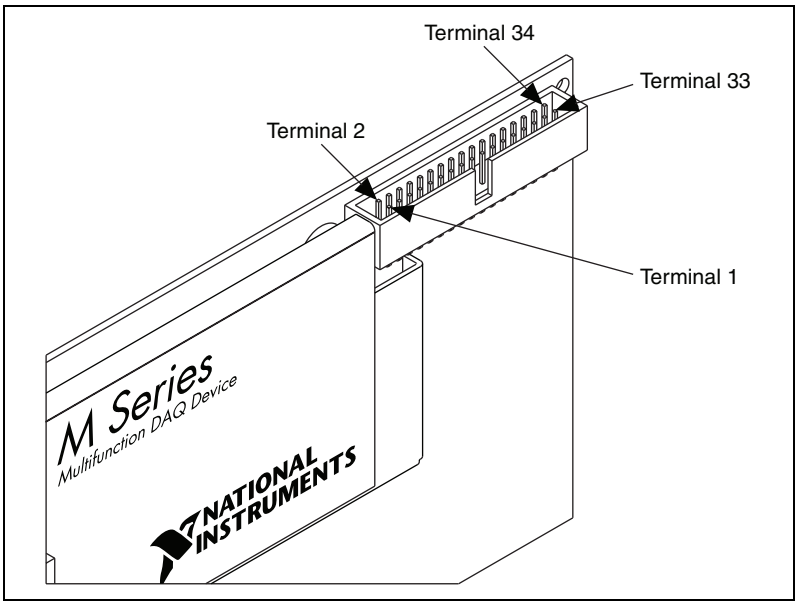


Figure 9-2. M Series PCI/PCI Express Device RTSI Pinout

Table 9-1. RTSI Signals

RTSI Bus Signal	Terminal
RTSI 7	34
RTSI 6	32
RTSI 5	30
RTSI 4	28
RTSI 3	26
RTSI 2	24
RTSI 1	22
RTSI 0	20
Not Connected. Do not connect signals to these terminals.	1–18
D GND	19, 21, 23, 25, 27, 29, 31, 33

Using RTSI as Outputs

RTSI <0..7> are bidirectional terminals. As an output, you can drive any of the following signals to any RTSI terminal:

- ai/StartTrigger
- ai/ReferenceTrigger
- ai/ConvertClock*
- ai/SampleClock
- ai/PauseTrigger
- ao/SampleClock*
- ao/StartTrigger
- ao/PauseTrigger
- 10 MHz Reference Clock
- Counter *n* Source, Gate, Z, Internal Output
- Change Detection Event
- Analog Comparison Event
- FREQ OUT
- PFI <0..5>

Note Signals with a * are inverted before being driven on the RTSI terminals.

Using RTSI Terminals as Timing Input Signals

You can use RTSI terminals to route external timing signals to many different M Series functions. Each RTSI terminal can be routed to any of the following signals:

- AI Convert Clock
- AI Sample Clock
- AI Start Trigger
- AI Reference Trigger
- AI Pause Trigger
- AI Sample Clock Timebase
- AO Start Trigger
- AO Sample Clock
- AO Sample Clock Timebase
- AO Pause Trigger

- Counter input signals for either counter—Source, Gate, Aux, HW_Arm, A, B, or Z
- DI Sample Clock
- DO Sample Clock

Most functions allow you to configure the polarity of PFI inputs and whether the input is edge or level sensitive.

RTSI Filters

You can enable a programmable debouncing filter on each PFI, RTSI, or PXI_STAR signal. When the filters are enabled, your device samples the input on each rising edge of a filter clock. M Series devices use an onboard oscillator to generate the filter clock with a 40 MHz frequency.

Note NI-DAQmx *only* supports filters on counter inputs.

The following is an example of low to high transitions of the input signal. High to low transitions work similarly.

Assume that an input terminal has been low for a long time. The input terminal then changes from low to high, but glitches several times. When the filter clock has sampled the signal high on N consecutive edges, the low to high transition is propagated to the rest of the circuit. The value of N depends on the filter setting; refer to Table 9-2.

Table 9-2. Filters

Filter Setting	N (Filter Clocks Needed to Pass Signal)	Pulse Width Guaranteed to Pass Filter	Pulse Width Guaranteed to Not Pass Filter
125 ns	5	125 ns	100 ns
6.425 µs	257	6.425 µs	6.400 µs
2.56 ms	~101,800	2.56 ms	2.54 ms
Disabled	—	—	—

The filter setting for each input can be configured independently. On power up, the filters are disabled. Figure 9-3 shows an example of a low to high transition on an input that has its filter set to 125 ns (N = 5).

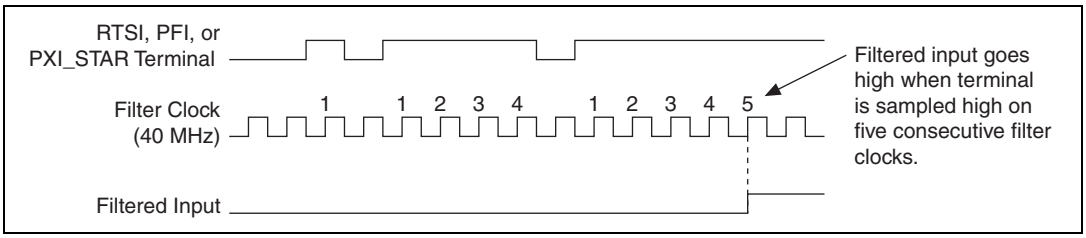


Figure 9-3. Filter Example

Enabling filters introduces jitter on the input signal. For the 125 ns and 6.425 µs filter settings, the jitter is up to 25 ns. On the 2.56 ms setting, the jitter is up to 10.025 µs.

When a PFI input is routed directly to RTSI, or a RTSI input is routed directly to PFI, the M Series device does not use the filtered version of the input signal.

Refer to the KnowledgeBase document, *Digital Filtering with M Series*, for more information about digital filters and counters. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rddfms`.

PXI Clock and Trigger Signals

Note PXI clock and trigger signals are only available on PXI/PXI Express devices.

PXI_CLK10

PXI_CLK10 is a common low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis.

PXI Triggers

A PXI chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

On M Series devices, the eight PXI trigger signals are synonymous with RTSI <0..7>.

Note that in a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI system, the Star Trigger bus implements a dedicated trigger line between the first peripheral slot (adjacent to the system slot) and the other peripheral slots. The Star Trigger can be used to synchronize multiple devices or to share a common trigger signal among devices.

A Star Trigger controller can be installed in this first peripheral slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this first peripheral slot.

An M Series device receives the Star Trigger signal (PXI_STAR) from a Star Trigger controller. PXI_STAR can be used as an external source for many AI, AO, and counter signals.

An M Series device is not a Star Trigger controller. An M Series device may be used in the first peripheral slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXI_STAR Filters

You can enable a programmable debouncing filter on each PFI, RTSI, or PXI_STAR signal. When the filters are enabled, your device samples the input on each rising edge of a filter clock. M Series devices use an onboard oscillator to generate the filter clock with a 40 MHz frequency.

Note NI-DAQmx *only* supports filters on counter inputs.

The following is an example of low to high transitions of the input signal. High to low transitions work similarly.

Assume that an input terminal has been low for a long time. The input terminal then changes from low to high, but glitches several times. When the filter clock has sampled the signal high on N consecutive edges, the low to high transition is propagated to the rest of the circuit. The value of N depends on the filter setting; refer to Table 9-3.

Table 9-3. Filters

Filter Setting	N (Filter Clocks Needed to Pass Signal)	Pulse Width Guaranteed to Pass Filter	Pulse Width Guaranteed to Not Pass Filter
125 ns	5	125 ns	100 ns
6.425 µs	257	6.425 µs	6.400 µs
2.56 ms	~101,800	2.56 ms	2.54 ms
Disabled	—	—	—

The filter setting for each input can be configured independently. On power up, the filters are disabled. Figure 9-4 shows an example of a low to high transition on an input that has its filter set to 125 ns (N = 5).

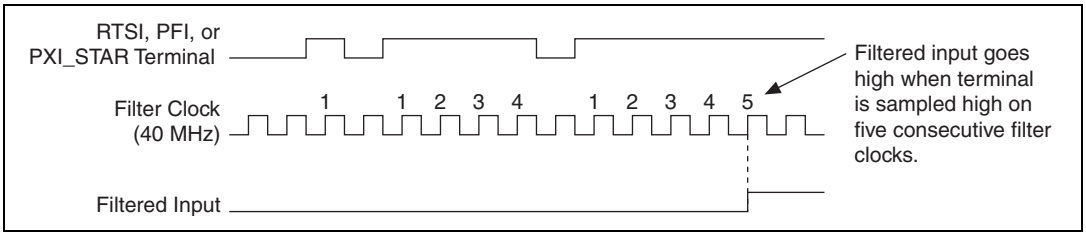


Figure 9-4. Filter Example

Enabling filters introduces jitter on the input signal. For the 125 ns and 6.425 µs filter settings, the jitter is up to 25 ns. On the 2.56 ms setting, the jitter is up to 10.025 µs.

When a PFI input is routed directly to RTSI, or a RTSI input is routed directly to PFI, the M Series device does not use the filtered version of the input signal.

Refer to the KnowledgeBase document, *Digital Filtering with M Series*, for more information about digital filters and counters. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rddfms`.

10

Bus Interface

The bus interface circuitry of M Series devices efficiently moves data between host memory and the measurement and acquisition circuits. M Series devices are available for the following platforms:

- PCI
- PCI Express
- PXI
- PXI Express
- USB

All M Series devices are jumperless for complete plug-and-play operation. The operating system automatically assigns the base address, interrupt levels, and other resources.

NI M Series PCI/PCIe/PXI/PXIe devices incorporate PCI-MITE technology to implement a high-performance PCI interface. M Series USB devices incorporate USB-STC2 technology to implement a Hi-Speed USB interface.

DMA Controllers and USB Signal Stream

NI M Series PCI/PCIe/PXI/PXIe devices have six fully-independent DMA controllers for high-performance transfers of data blocks. One DMA controller is available for each measurement and acquisition block:

- Analog input
- Analog output
- Counter 0
- Counter 1
- Digital waveform generation (digital output)
- Digital waveform acquisition (digital input)

Each DMA controller channel contains a FIFO and independent processes for filling and emptying the FIFO. This allows the buses involved in the transfer to operate independently for maximum performance. Data is

transferred simultaneously between the ports. The DMA controller supports burst transfers to and from the FIFO.

Each DMA controller supports several features to optimize PCI/PXI bus utilization. The DMA controllers pack and unpack data through the FIFOs. This feature allows the DMA controllers to combine multiple 16-bit transfers to the DAQ circuitry into a single 32-bit burst transfer on PCI. The DMA controllers also automatically handle unaligned memory buffers on PCI/PXI.

M Series USB devices have four fully-independent USB Signal Stream for high-performance transfers of data blocks. These channels are assigned to the first four measurement/acquisition circuits that request one.

PXI Considerations

Note PXI clock and trigger signals are only available on PXI devices.

PXI Clock and Trigger Signals

Refer to the *PXI_CLK10*, *PXI Triggers*, *PXI_STAR Trigger*, and *PXI_STAR Filters* sections of Chapter 9, *Digital Routing and Clock Generation*, for more information about PXI clock and trigger signals.

PXI and PXI Express

NI PXI M Series devices can be installed in any PXI chassis and most slots of PXI Express hybrid chassis. NI PXI Express M Series devices can be installed in any PXI Express slot in PXI Express chassis.

PXI specifications are developed by the PXI System Alliance (`www.pxisa.org`). Using the terminology of the PXI specifications, some NI PXI M Series devices are *3U Hybrid Slot-Compatible PXI-1 Peripheral Modules*. Refer to your device specifications to see if your PXI M Series device is hybrid slot-compatible.

3U designates devices that are 100 mm tall (as opposed to the taller 6U modules).

Hybrid slot-compatible defines where the device can be installed. PXI M Series devices can be installed in the following chassis and slots:

- **PXI chassis**—PXI M Series devices can be installed in any peripheral slot of a PXI chassis.

- **PXI Express chassis**[1]—PXI M Series devices can be installed in the following PXI Express chassis slots:
  - **PXI-1 slots**—Accepts all PXI modules
  - **PXI hybrid slots**—Accepts PXI modules that are hybrid slot-compatible or PXI Express modules
  - **PXI Express slots**—Accepts PXI Express modules

PXI-1 devices use PCI signaling to communicate to the host controller (as opposed to PCI Express signaling).

Peripheral devices are installed in peripheral slots and are not system controllers.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by the *PXI Hardware Specification Revision 2.1*. If you use a PXI-compatible plug-in module in a standard CompactPCI chassis, you cannot use PXI-specific functions, but you can still use the basic plug-in device functions. For example, the RTSI bus on a PXI M Series device is available in a PXI chassis, but not in a CompactPCI chassis.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. The PXI M Series device works in any standard CompactPCI chassis adhering to the *PICMG CompactPCI 2.0 R3.0* core specification.

PXI-specific features are implemented on the J2 connector of the CompactPCI bus. The PXI device is compatible with any CompactPCI chassis with a sub-bus that does not drive the lines used by that device. Even if the sub-bus is capable of driving these lines, the PXI device is still compatible as long as those terminals on the sub-bus are disabled by default and never enabled.

Caution Damage can result if these lines are driven by the sub-bus. NI is *not* liable for any damage resulting from improper signal connections.

[1] For some PXI M Series devices, there are two variants—one that will work in PXI hybrid slots and one that supports local bus for SCXI control when the device is in the right-most slot. Refer to the device specifications for more information.

Data Transfer Methods

(NI PCI/PCIe/PXI/PXIe Devices) The three primary ways to transfer data across the PCI bus are direct memory access (DMA), interrupt request (IRQ), and programmed I/O:

- **Direct Memory Access (DMA)**—DMA is a method to transfer data between the device and computer memory without the involvement of the CPU. This method makes DMA the fastest available data transfer method. NI uses DMA hardware and software technology to achieve high throughput rates and increase system utilization. DMA is the default method of data transfer for PCI/PCIe/PXI/PXIe devices.
- **Interrupt Request (IRQ)**—IRQ transfers rely on the CPU to service data transfer requests. The device notifies the CPU when it is ready to transfer data. The data transfer speed is tightly coupled to the rate at which the CPU can service the interrupt requests. If you are using interrupts to transfer data at a rate faster than the rate the CPU can service the interrupts, your systems may start to freeze.
- **Programmed I/O**—Programmed I/O is a data transfer mechanism where the user's program is responsible for transferring data. Each read or write call in the program initiates the transfer of data. Programmed I/O is typically used in software-timed (on-demand) operations. Refer to the *Software-Timed Generations* section of Chapter 5, *Analog Output*, for more information.

(USB Devices) The two primary ways to transfer data across the USB bus are USB Signal Stream and programmed I/O:

- **USB Signal Stream**—USB Signal Stream is a method to transfer data between the device and computer memory using USB bulk transfers without intervention of the microcontroller on the NI device. NI uses USB Signal Stream hardware and software technology to achieve high throughput rates and increase system utilization in USB devices.
- **Programmed I/O**—Programmed I/O is a data transfer mechanism where the user's program is responsible for transferring data. Each read or write call in the program initiates the transfer of data. Programmed I/O is typically used in software-timed (on-demand) operations. Refer to the *Software-Timed Generations* section of Chapter 5, *Analog Output*, for more information.

Changing Data Transfer Methods

(NI PCI/PCIe/PXI/PXIe Devices) On PCI, PCI Express, PXI, and PXI Express M Series devices, each measurement and acquisition circuit (that is, AI, AO, and so on) has a dedicated DMA channel. So in most applications, all data transfers use DMA.

However, NI-DAQmx allows you to disable DMA and use interrupts. To change your data transfer mechanism between DMA and interrupts in NI-DAQmx, use the **Data Transfer Mechanism** property node.

(USB Devices) USB M Series devices have four dedicated USB Signal Stream channels. These channels are assigned to the first four measurement/acquisition circuits that request one. If a USB Signal Stream is not available, you must set the data transfer mechanism to programmed I/O; otherwise the driver returns an error. To change your data transfer mechanism between USB Signal Stream and programmed I/O, use the **Data Transfer Mechanism** property node function in NI-DAQmx.

11

Triggering

A *trigger* is a signal that causes an action, such as starting or stopping the acquisition of data. When you configure a trigger, you must decide how you want to produce the trigger and the action you want the trigger to cause. All M Series devices support internal software triggering, as well as external digital triggering. Some devices also support analog triggering. For information about the different actions triggers can perform for each sub-system of the device, refer to the following sections:

- The *Analog Input Triggering* section of Chapter 4, *Analog Input*
- The *Analog Output Triggering* section of Chapter 5, *Analog Output*
- The *Counter Triggering* section of Chapter 7, *Counters*

Note Not all M Series devices support analog triggering. For more information about triggering compatibility, refer to the specifications document for your device.

Triggering with a Digital Source

Your DAQ device can generate a trigger on a digital signal. You must specify a source and an edge. The digital source can be any of the PFI, RTSI, or PXI_STAR signals.

The edge can be either the rising edge or falling edge of the digital signal. A rising edge is a transition from a low logic level to a high logic level. A falling edge is a high to low transition.

Figure 11-1 shows a falling-edge trigger.

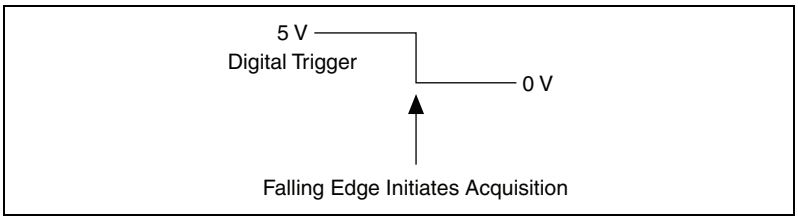


Figure 11-1. Falling-Edge Trigger

You also can program your DAQ device to perform an action in response to a trigger from a digital source. The action can affect the following:

- Analog input acquisition
- Analog output generation
- Counter behavior
- Digital waveform acquisition and generation

Triggering with an Analog Source

Some M Series devices can generate a trigger on an analog signal. To find your device triggering options, refer to the specifications document for your device.

Figure 11-2 shows the analog trigger circuit.

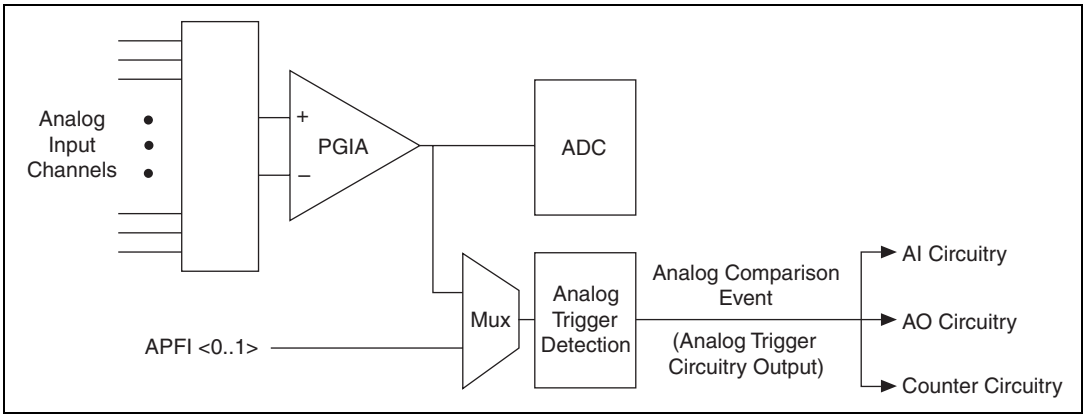


Figure 11-2. Analog Trigger Circuit

You must specify a source and an analog trigger type. The source can be either an APFI <0..1> terminal or an analog input channel.

APFI <0..1> Terminals

When you use either APFI <0..1> terminal as an analog trigger, you should drive the terminal with a low-impedance signal source (less than 1 kΩ source impedance). If APFI <0..1> are left unconnected, they are susceptible to crosstalk from adjacent terminals, which can cause false triggering. Note that the APFI <0..1> terminals also can be used for other functions such as the AO External Reference input, as described in the *AO Offset and AO Reference Selection* section of Chapter 5, *Analog Output*.

Analog Input Channels

Select any analog input channel to drive the NI-PGIA. The NI-PGIA amplifies the signal as determined by the input ground-reference setting and the input range. The output of the NI-PGIA then drives the analog trigger detection circuit. By using the NI-PGIA, you can trigger on very small voltage changes in the input signal.

When the DAQ device is waiting for an analog trigger with a AI channel as the source, the AI muxes should not route different AI channels to the NI-PGIA. If a different channel is routed to the NI-PGIA, the trigger condition on the desired channel could be missed. The other channels also could generate false triggers.

This behavior places some restrictions on using AI channels as trigger sources. When you use an analog start trigger, the trigger channel must be the first channel in the channel list. When you use an analog reference or pause trigger, and the analog channel is the source of the trigger, there can be only one channel in the channel list.

Analog Trigger Actions

The output of the analog trigger detection circuit is the *Analog Comparison Event* signal. You can program your DAQ device to perform an action in response to the Analog Comparison Event signal. The action can affect the following:

- Analog input acquisition
- Analog output generation
- Counter behavior

Routing Analog Comparison Event to an Output Terminal

You can route Analog Comparison Event out to any PFI <0..15> or RTSI <0..7> terminal.

Analog Trigger Types

Configure the analog trigger circuitry to different triggering modes—analog edge triggering, analog edge triggering with hysteresis, or analog window triggering.

Analog Edge Triggering

Configure the analog trigger circuitry to detect when the analog signal is below or above a level you specify.

In below-level analog triggering mode, shown in Figure 11-3, the trigger is generated when the signal value is less than Level.

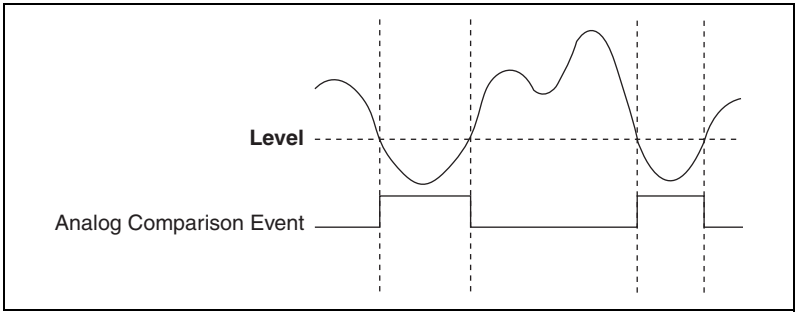


Figure 11-3. Below-Level Analog Triggering Mode

In above-level analog triggering mode, shown in Figure 11-4, the trigger is generated when the signal value is greater than Level.

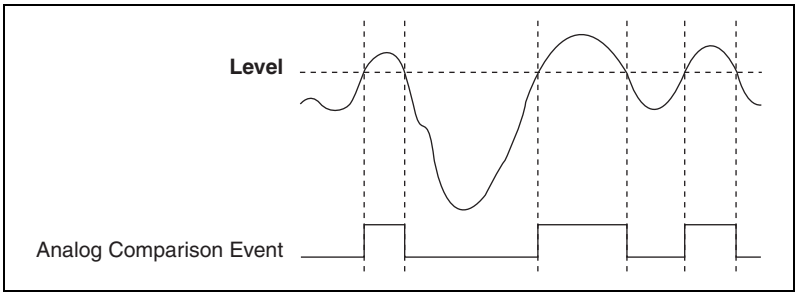


Figure 11-4. Above-Level Analog Triggering Mode

Analog Edge Triggering with Hysteresis

Hysteresis adds a programmable voltage region above or below the trigger level that an input signal must pass through before the DAQ device recognizes a trigger condition, and is often used to reduce false triggering due to noise or jitter in the signal.

Analog Edge Trigger with Hysteresis (Rising Slope)

When using hysteresis with a rising slope, you specify a trigger level and amount of hysteresis. The *high threshold* is the trigger level; the *low threshold* is the trigger level minus the hysteresis.

For the trigger to assert, the signal must first be below the low threshold, then go above the high threshold. The trigger stays asserted until the signal returns below the low threshold. The output of the trigger detection circuitry is the internal Analog Comparison Event signal, as shown in Figure 11-5.

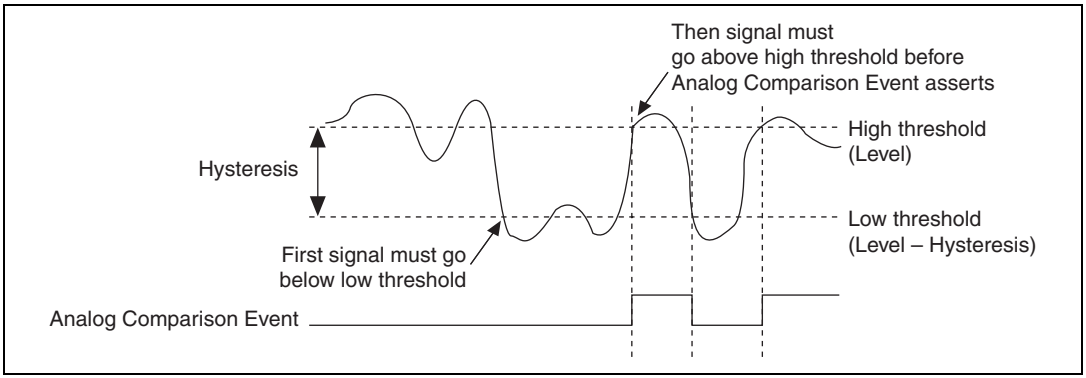


Figure 11-5. Analog Edge Triggering with Hysteresis Rising Slope Example

Analog Edge Trigger with Hysteresis (Falling Slope)

When using hysteresis with a falling slope, you specify a trigger level and amount of hysteresis. The low threshold is the trigger level; the high threshold is the trigger level plus the hysteresis.

For the trigger to assert, the signal must first be above the high threshold, then go below the low threshold. The trigger stays asserted until the signal returns above the high threshold. The output of the trigger detection circuitry is the internal Analog Comparison Event signal, as shown in Figure 11-6.

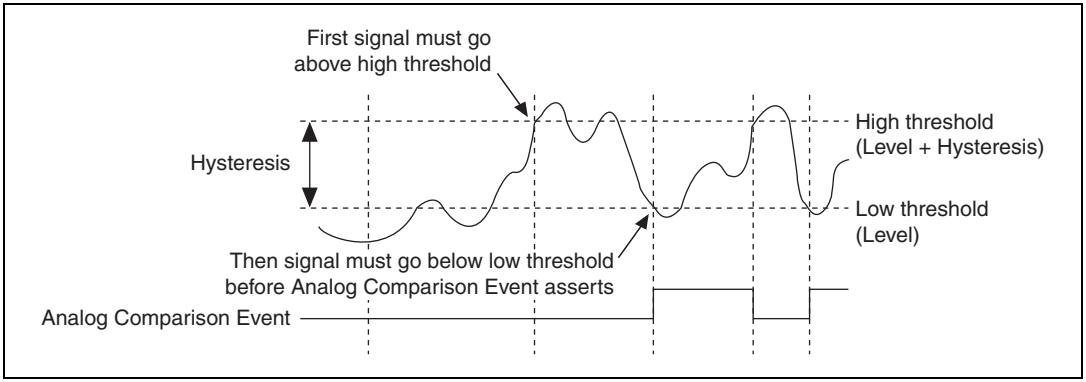


Figure 11-6. Analog Edge Triggering with Hysteresis Falling Slope Example

Analog Window Triggering

An analog window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two voltage levels. Specify the levels by setting the window Top value and the window Bottom value.

Figure 11-7 demonstrates a trigger that asserts when the signal enters the window.

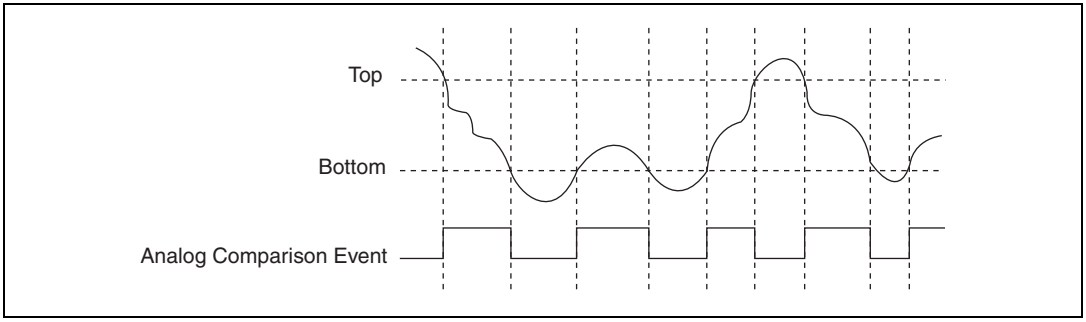


Figure 11-7. Analog Window Triggering Mode (Entering Window)

Analog Trigger Accuracy

The analog trigger circuitry compares the voltage of the trigger source to the output of programmable trigger DACs. When you configure the level (or the high and low limits in window trigger mode), the device adjusts the output of the trigger DACs. Refer to the specifications document for your device to find the accuracy or resolution of these DACs, which also shows the accuracy or resolution of analog triggers.

To improve accuracy, do the following:

- Use an AI channel (with a small input range) instead of APFI <0..1> as your trigger source. The DAQ device does not amplify the APFI <0..1> signals. When using an AI channel, the NI-PGIA amplifies the AI channel signal before driving the analog trigger circuitry. If you configure the AI channel to have a small input range, you can trigger on very small voltage changes in the input signal.
- Software-calibrate the analog trigger circuitry. The propagation delay from when a valid trigger condition is met to when the analog trigger circuitry emits the Analog Comparison Event may have an impact on your measurements if the trigger signal has a high slew rate. If you find these conditions have a noticeable impact on your measurements, you can perform software calibration on the analog trigger circuitry by configuring your task as normal and applying a known signal for your analog trigger. Comparing the observed results against the expected results, you can calculate the necessary offsets to apply in software to fine-tune the desired triggering behavior.

A

Device-Specific Information

This appendix contains device pinouts, specifications, cable and accessory choices, and other information for the following M Series devices.

- NI 6220
- NI 6221
- NI 6224
- NI 6225
- NI 6229
- NI 6250
- NI 6251
- NI 6254
- NI 6255
- NI 6259
- NI 6280
- NI 6281
- NI 6284
- NI 6289

To obtain documentation for devices not listed here, refer to `ni.com/manuals`.

NI 6220

PCI/PXI-6220 Pinout

Figure A-1 shows the pinout of the PCI/PXI-6220.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

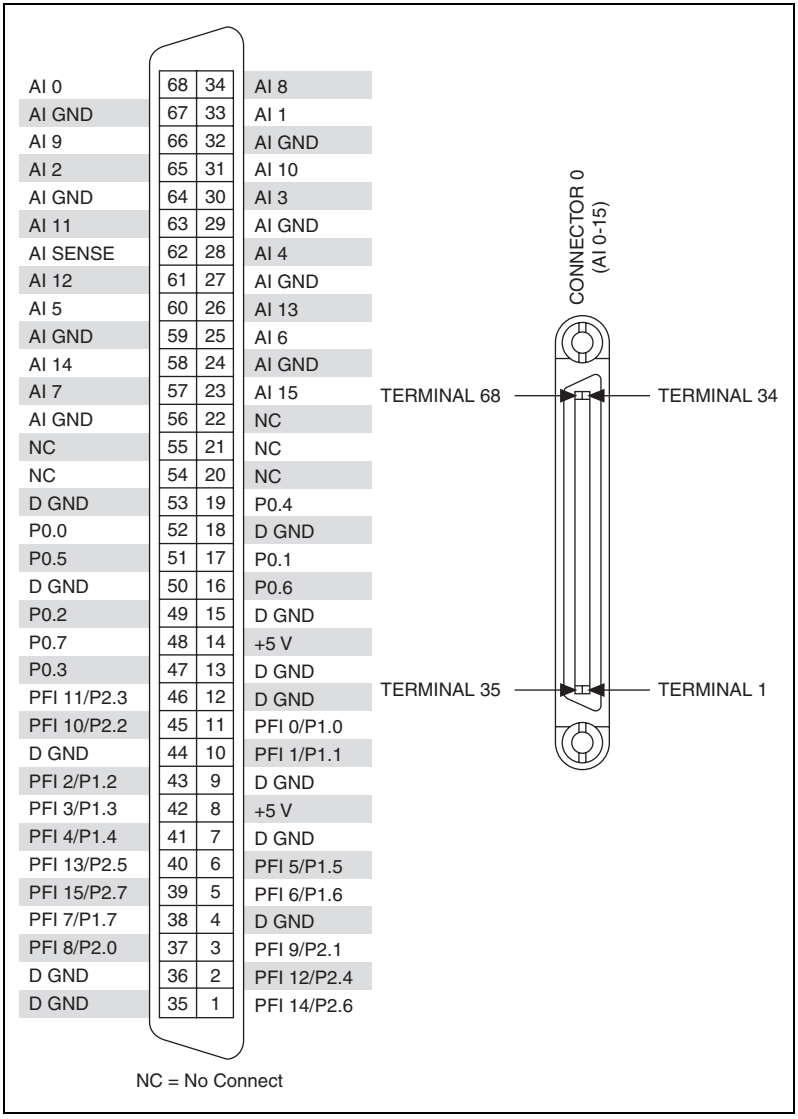


Figure A-1. PCI/PXI-6220 Pinout

Table A-1. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6220 Specifications

Refer to the *NI 622x Specifications* for more detailed information about the PCI/PXI-6220 device.

PCI/PXI-6220 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the PCI/PXI-6220. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706 front panel mounted terminal block for PXI M Series devices

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

NI 6221

The following sections contain information about the PCI/PXI-6221 (68-pin), PCI-6221 (37-pin), USB-6221 Screw Terminal, and USB-6221 BNC devices.

PCI/PXI-6221 (68-Pin)

PCI/PXI-6221 (68-Pin) Pinout

Figure A-2 shows the pinout of the PCI/PXI-6221 (68-pin) device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

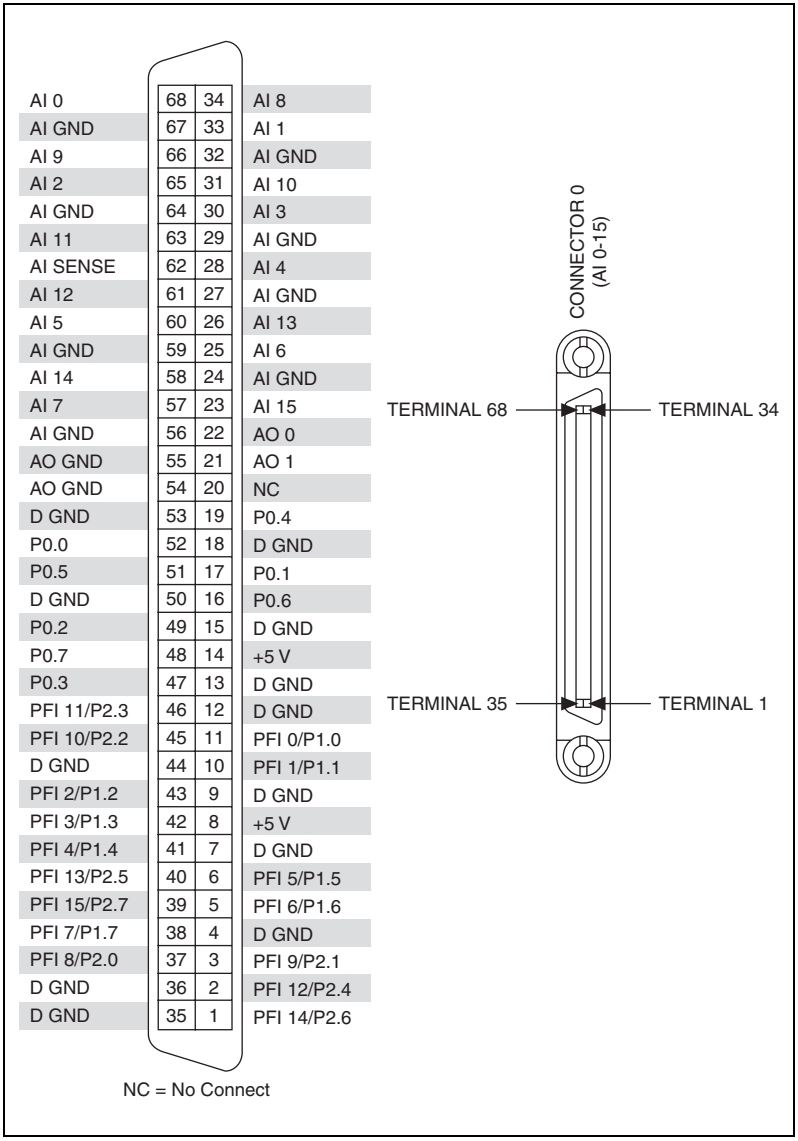


Figure A-2. PCI/PXI-6221 (68-Pin) Pinout

Table A-2. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6221 (68-Pin) Specifications

Refer to the *NI 622x Specifications* for more detailed information about the PCI/PXI-6221 (68-pin) device.

PCI/PXI-6221 (68-Pin) Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the PCI/PXI-6221 (68-pin). Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706 front panel mounted terminal block for PXI M Series devices

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

PCI-6221 (37-Pin)

PCI-6221 (37-Pin) Pinout

Figure A-3 shows the pinout of the PCI-6221 (37-pin) device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

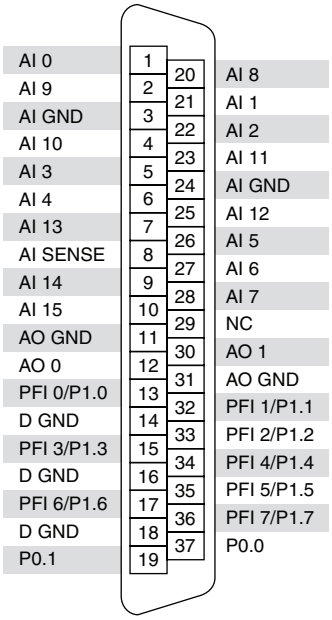


Figure A-3. PCI-6221 (37-Pin) Pinout

Table A-3. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	13 (PFI 0)
CTR 0 GATE	32 (PFI 1)
CTR 0 AUX	33 (PFI 2)
CTR 0 OUT	17 (PFI 6)
CTR 0 A	13 (PFI 0)
CTR 0 Z	32 (PFI 1)
CTR 0 B	33 (PFI 2)
CTR 1 SRC	15 (PFI 3)
CTR 1 GATE	34 (PFI 4)
CTR 1 AUX	35 (PFI 5)
CTR 1 OUT	36 (PFI 7)
CTR 1 A	15 (PFI 3)
CTR 1 Z	34 (PFI 4)
CTR 1 B	35 (PFI 5)
FREQ OUT	35 (PFI 5)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI-6221 (37-Pin) Specifications

Refer to the *NI 622x Specifications* for more detailed information about the PCI-6221 (37-pin) device.

PCI-6221 (37-Pin) Accessory and Cabling Options

This section describes some cable and accessory options for the PCI-6221 (37-pin) device. Refer to `ni.com` for other accessory options, including new devices.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH37F-37M cable to connect a PCI-6221 (37-pin) device to a connector block, such as the following:

- **CB-37FH**—DIN-mountable connector block with 37 screw terminals
- **CB-37F-LP**—Low profile connector block with 37 screw terminals

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices.

Cables

In most applications, you can use the following cables:

- **SH37F-37M-1**—37-pin female-to-male shielded I/O cable, 1 m
- **SH37F-37M-2**—37-pin female-to-male shielded I/O cable, 2 m

Custom Cabling and Connectivity

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6221 Screw Terminal

USB-6221 Screw Terminal Pinout

Figure A-4 shows the pinout of the USB-6221 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

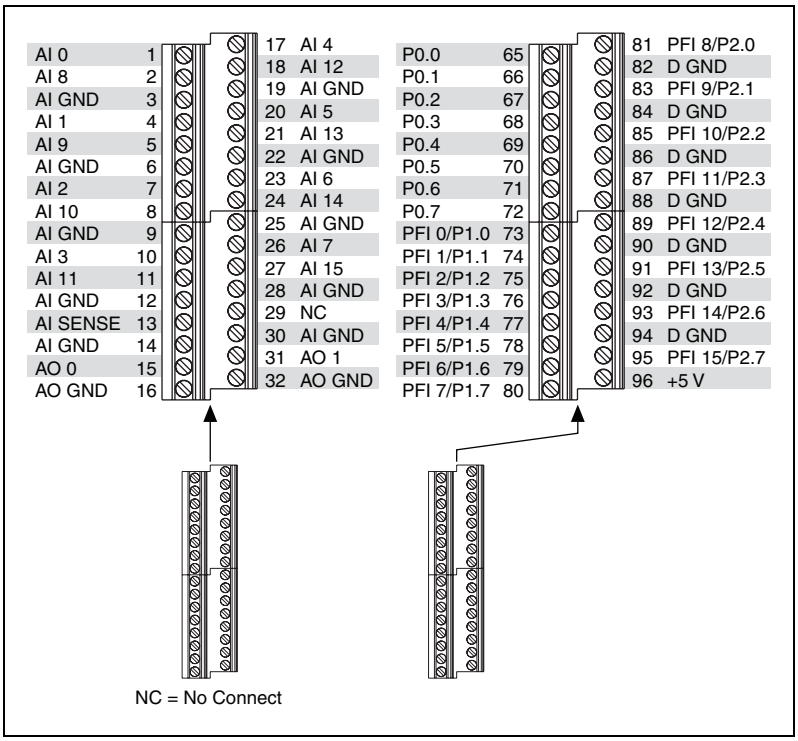


Figure A-4. USB-6221 Screw Terminal Pinout

Table A-4. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	81 (PFI 8)
CTR 0 GATE	83 (PFI 9)
CTR 0 AUX	85 (PFI 10)
CTR 0 OUT	89 (PFI 12)
CTR 0 A	81 (PFI 8)

Table A-4. Default NI-DAQmx Counter/Timer Pins (Continued)

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 Z	83 (PFI 9)
CTR 0 B	85 (PFI 10)
CTR 1 SRC	76 (PFI 3)
CTR 1 GATE	77 (PFI 4)
CTR 1 AUX	87 (PFI 11)
CTR 1 OUT	91 (PFI 13)
CTR 1 A	76 (PFI 3)
CTR 1 Z	77 (PFI 4)
CTR 1 B	87 (PFI 11)
FREQ OUT	93 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6221 Screw Terminal Specifications

Refer to the *NI 622x Specifications* for more detailed information about the USB-6221 Screw Terminal device.

USB-6221 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6221 Screw Terminal LEDs.

USB-6221 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6221 Screw Terminal.

USB-6221 BNC

USB-6221 BNC Pinout

Figure A-5 shows the pinout of the USB-6221 BNC.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

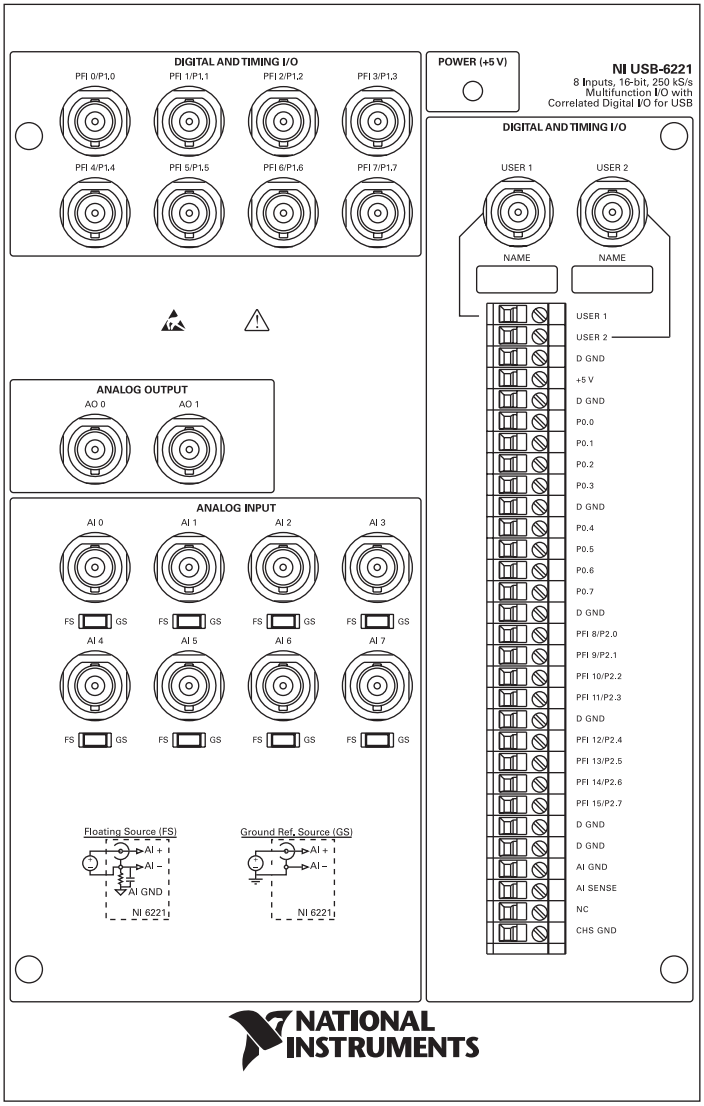


Figure A-5. USB-6221 BNC Top Panel and Pinout

Table A-5. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Name
CTR 0 SRC	PFI 8
CTR 0 GATE	PFI 9
CTR 0 AUX	PFI 10
CTR 0 OUT	PFI 12
CTR 0 A	PFI 8
CTR 0 Z	PFI 9
CTR 0 B	PFI 10
CTR 1 SRC	PFI 3
CTR 1 GATE	PFI 4
CTR 1 AUX	PFI 11
CTR 1 OUT	PFI 13
CTR 1 A	PFI 3
CTR 1 Z	PFI 4
CTR 1 B	PFI 11
FREQ OUT	PFI 14

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Connecting Signals to the USB-6221 BNC

Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

Differential Signals

To connect differential signals, determine the type of signal source you are using—a floating signal (FS) source or a ground-referenced signal (GS) source. Refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*, for more information.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-6 shows the AI 0 BNC and corresponding FS/GS switch on the top panel of the USB-6221 BNC.

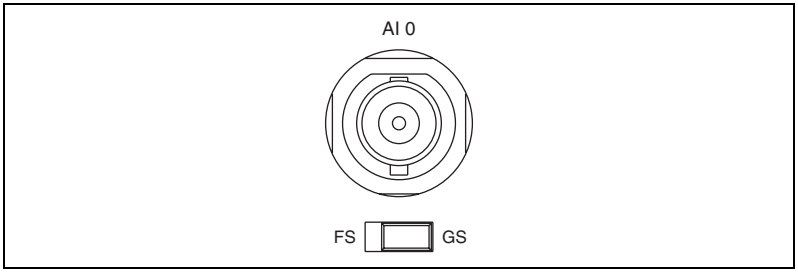


Figure A-6. FS/GS Switch

Figure A-7 shows the analog input circuitry on the USB-6221 BNC. When the switch is set to the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

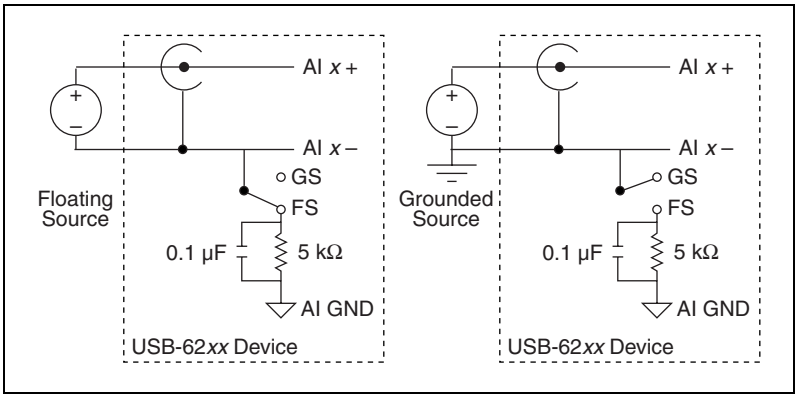


Figure A-7. Analog Input Circuitry

Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-8.

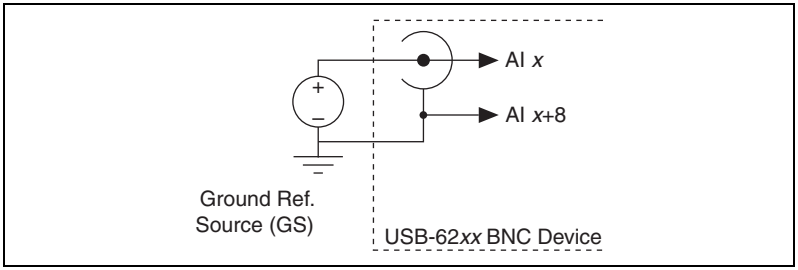


Figure A-8. Single-Ended Channels

When you set the source type to the GS position and configure the device for single-ended input in software, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 16 single-ended channels are available in single-ended measurement modes.

For information on how to connect your single-ended signals, AI GND, and/or AI SENSE, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*. For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-9 shows the analog output circuitry on the USB-6221 BNC.

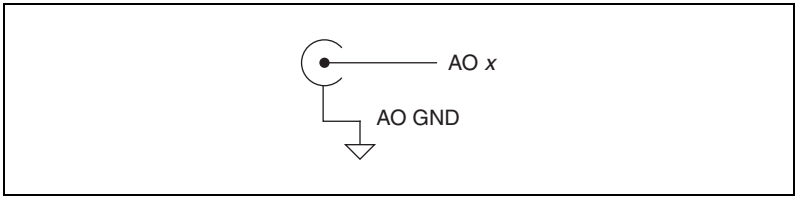


Figure A-9. Analog Output Circuitry

Refer to the *Connecting Analog Output Signals* section of Chapter 5, *Analog Output*, for more information.

Digital I/O and Timing I/O

You can access digital I/O and timing I/O signals on the BNC connectors labeled PFI <0..7>/P1.<0..7>. Figure A-10 shows the DIO/TIO circuitry on the USB-6221 BNC.

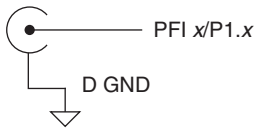


Figure A-10. Digital I/O and Timing I/O Circuitry

Refer to the *Connecting Digital I/O Signals* section of Chapter 6, *Digital I/O*, and the *Connecting PFI Input Signals* section of Chapter 8, *PFI*, for more information.

USER 1 and USER 2

The USER 1 and USER 2 BNC connectors allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 and USER 2 BNC connectors are routed (internal to the USB-6221 BNC) to the USER 1 and USER 2 screw terminals, as shown in Figure A-11.

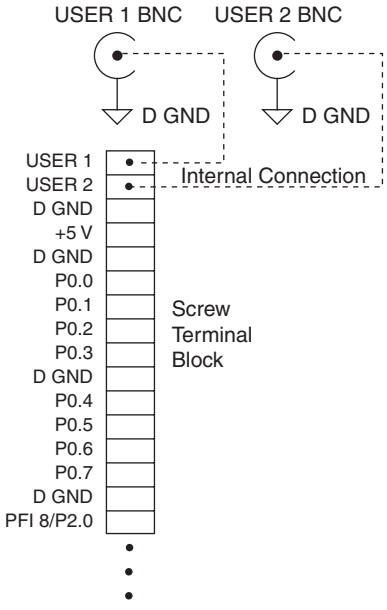


Figure A-11. USER 1 and USER 2 BNC Connections

Figure A-12 shows an example of how to use the USER 1 and USER 2 BNCs. To access the PFI 8 signal from a BNC, connect USER 1 on the screw terminal block to PFI 8 with a wire.

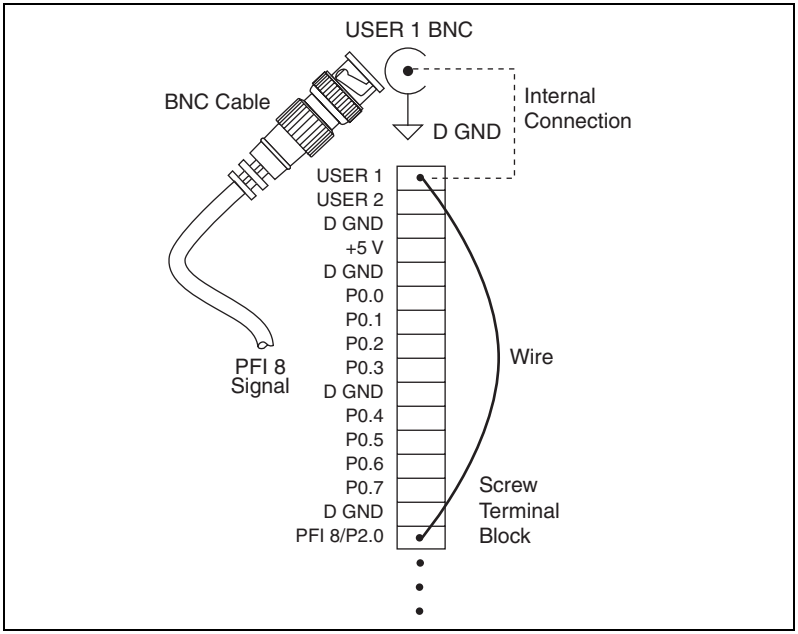


Figure A-12. Connecting PFI 8 to USER 1 BNC

The designated space below each USER <1..2> BNC is for marking or labeling signal names.

USB-6221 BNC Specifications

Refer to the *NI 622x Specifications* for more detailed information about the USB-6221 BNC device.

USB-6221 BNC LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6221 BNC LEDs.

USB-6221 BNC Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6221 BNC.

NI 6224

PCI/PXI-6224 Pinout

Figure A-13 shows the pinout of the PCI/PXI-6224. The I/O signals appear on two 68-pin connectors.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

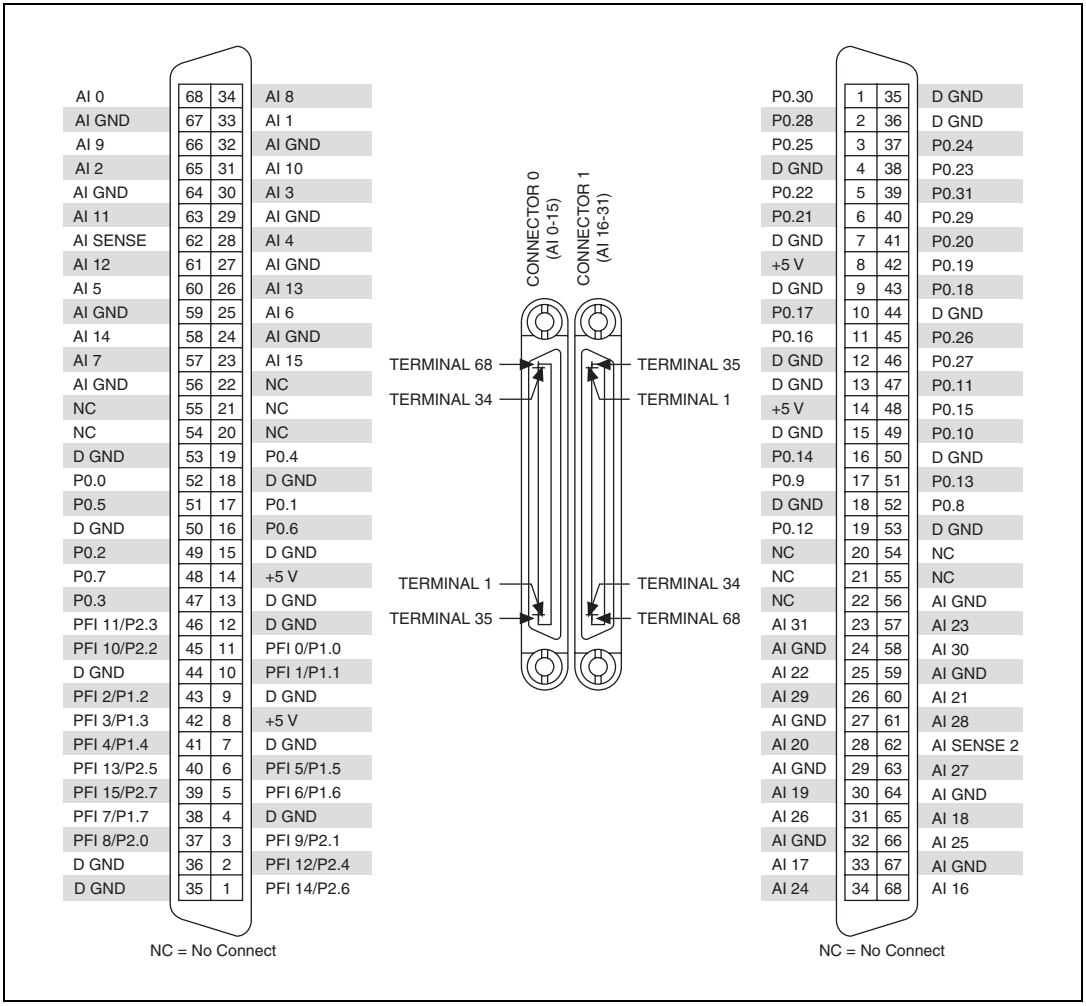


Figure A-13. PCI/PXI-6224 Pinout

Table A-6. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6224 Specifications

Refer to the *NI 622x Specifications* for more detailed information about the PCI/PXI-6224 device.

PCI/PXI-6224 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the PCI/PXI-6224. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. NI-DAQ 7.4 and later supports SCXI in parallel mode on Connector 1.

Note When using Connector 1 in parallel mode with SCXI modules that support track and hold, you must programmatically disable track and hold.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output

- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706[1] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

[1] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

NI 6225

The following sections contain information about the PCI/PXI-6225, USB-6225 Screw Terminal, and USB-6225 Mass Termination devices.

PCI/PXI-6225

PCI/PXI-6225 Pinout

Figure A-14 shows the pinout of the PCI/PXI-6225.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

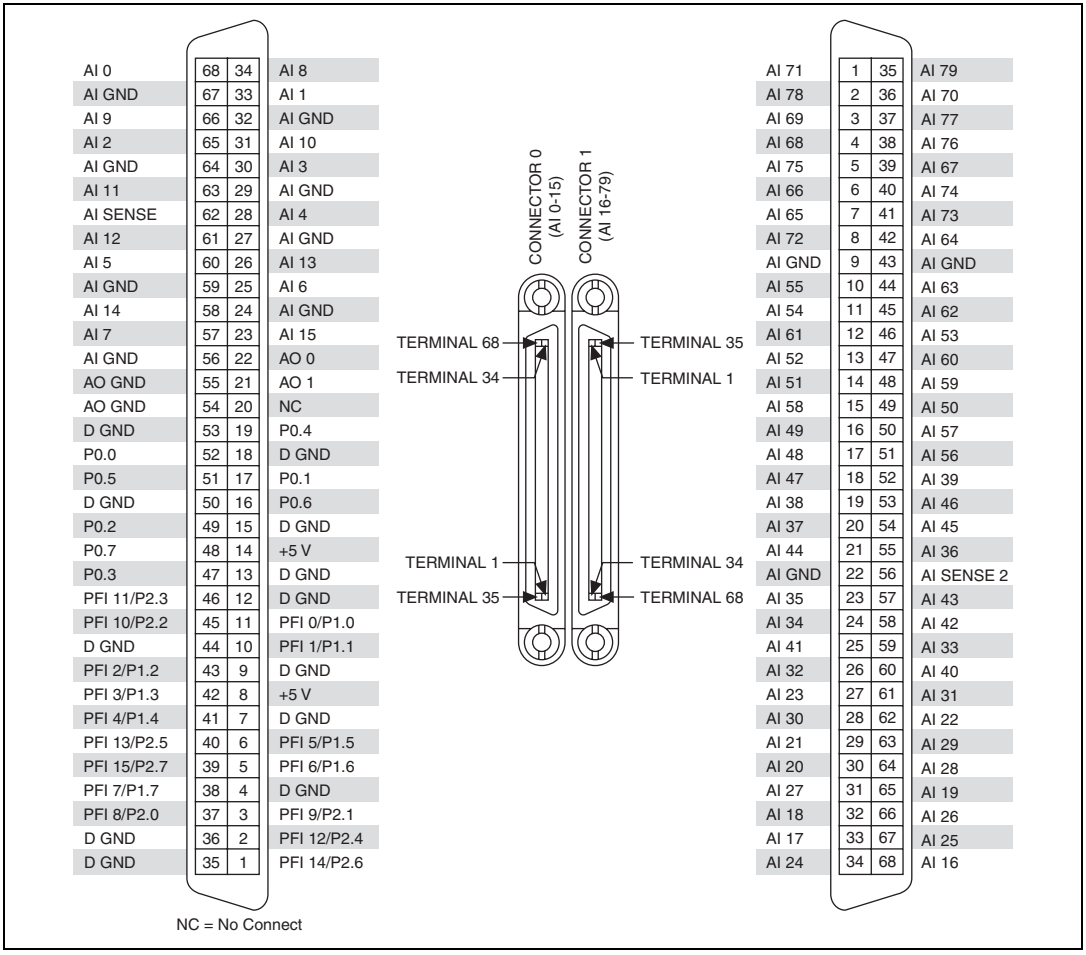


Figure A-14. PCI/PXI-6225 Pinout

Table A-7. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6225 Specifications

Refer to the *NI 622x Specifications* for more detailed information about the PCI/PXI-6225 device.

PCI/PXI-6225 Accessory and Cabling Options

This section describes some cable and accessory options for the PCI/PXI-6225. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. Connector 1 cannot be used to control SCXI.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. Connector 1 cannot be used with SCCs.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

Using a BNC Accessory with Connector 0

Connector 0 of your device is compatible with several BNC accessories:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use the SHC68-68-EPM shielded cable, to connect Connector 0 of your DAQ device to BNC accessories.

Using a BNC Accessory with Connector 1

Connector 1 of your device is compatible with BNC-2115. BNC-2115 provides BNC connectivity to 24 of the differential (48 single ended) analog input signals on Connector 1.

You can use an SHC68-68 cable to connect to the BNC-2115.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks such as:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor (make sure the switches are set properly)[1]
- TBX-68 DIN rail-mountable connector block
- TB-2706[2] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your PCI/PXI-6225 device. You can use two screw terminal accessories with one M Series device by using both connectors.[3]

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

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[1] NI recommends that you use the SHC68-68 cable when the SCB-68 is connected to Connector 1.

[2] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

[3] The SCC-68 only can be used with Connector 0.

Cables

The PCI/PXI-6225 has two connectors that require different cables.

Choosing a Cable for Connector 0

In most applications, you can use the following cables with Connector 0:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Choosing a Cable for Connector 1

In most applications, you can use the following cables with Connector 1:

- **SHC68-68**—Shielded cable with 34 twisted pairs of wire. Each differential analog input channel on Connector 1 is routed on a twisted pair on the SHC68-68 cable
- **RC68-68**—Highly flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6225 Screw Terminal

USB-6225 Screw Terminal Pinout

Figure A-15 shows the pinout of the USB-6225 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note For a ground connection, you can connect the shield of a shielded cable to the chassis ground lug, depicted in Figure A-15.

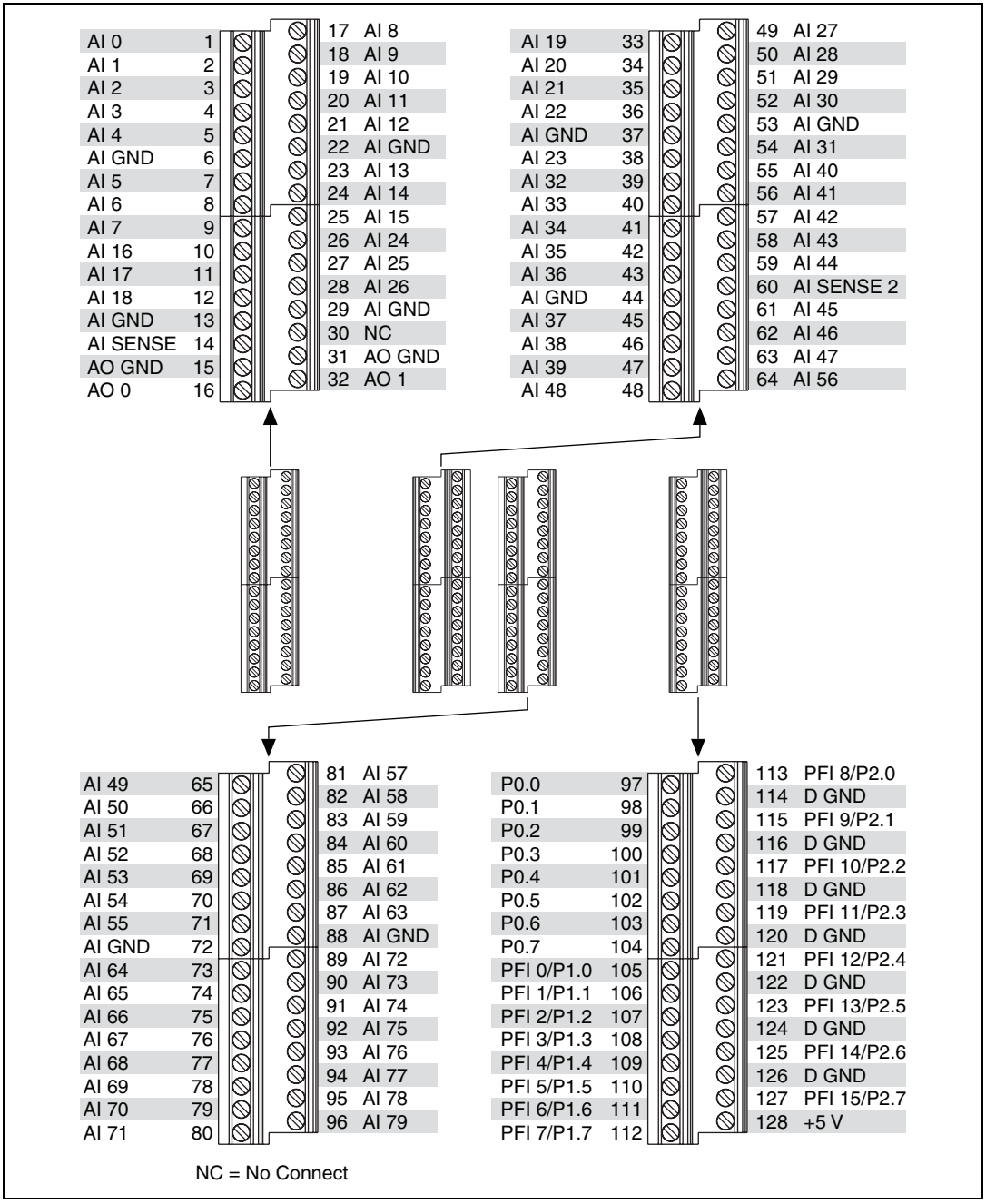

Figure A-15. USB-6225 Screw Terminal Pinout

Table A-8. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	113 (PFI 8)
CTR 0 GATE	115 (PFI 9)
CTR 0 AUX	117 (PFI 10)
CTR 0 OUT	121 (PFI 12)
CTR 0 A	113 (PFI 8)
CTR 0 Z	115 (PFI 9)
CTR 0 B	117 (PFI 10)
CTR 1 SRC	108 (PFI 3)
CTR 1 GATE	109 (PFI 4)
CTR 1 AUX	119 (PFI 11)
CTR 1 OUT	123 (PFI 13)
CTR 1 A	108 (PFI 3)
CTR 1 Z	109 (PFI 4)
CTR 1 B	119 (PFI 11)
FREQ OUT	125 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6225 Screw Terminal Specifications

Refer to the *NI 622x Specifications* for more detailed information about the USB-6225 Screw Terminal device.

USB-6225 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6225 Screw Terminal LEDs.

USB-6225 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6225 Screw Terminal.

USB-6225 Mass Termination

USB-6225 Mass Termination Pinout

Figure A-16 shows the pinout of the USB-6225 Mass Termination device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

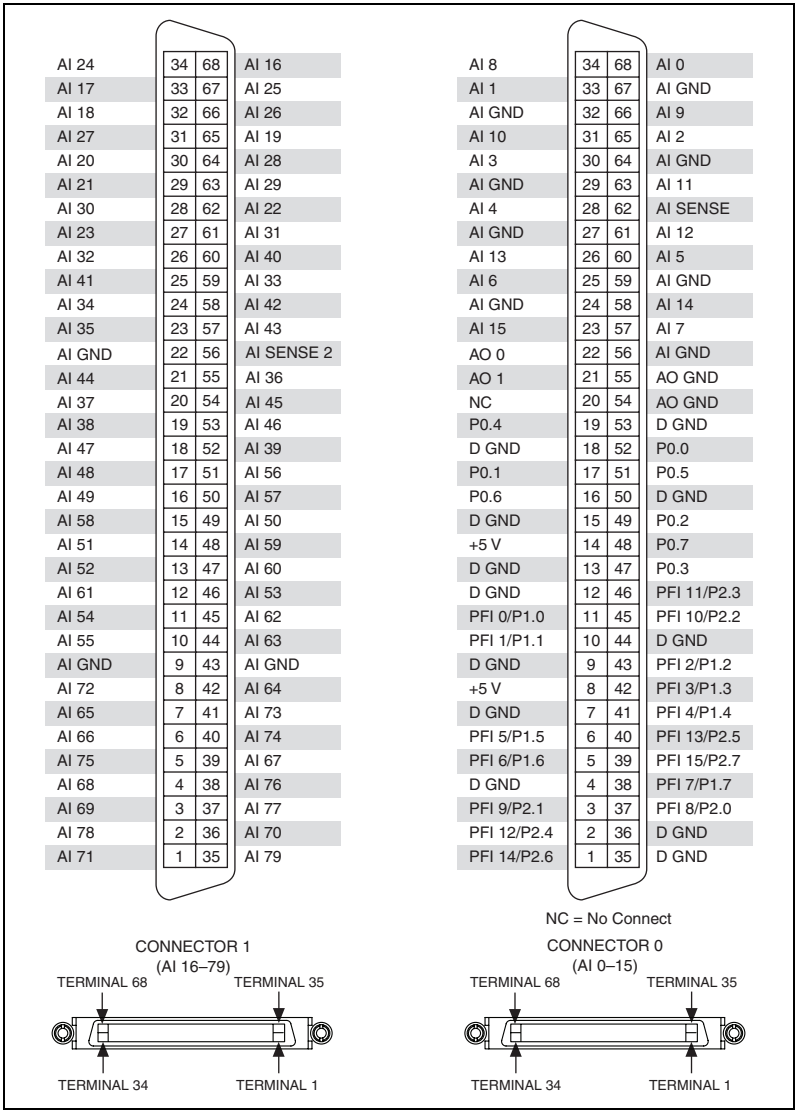

Figure A-16. USB-6225 Mass Termination Pinout

Table A-9. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6225 Mass Termination Specifications

Refer to the *NI 622x Specifications* for more detailed information about the USB-6225 Mass Termination device.

USB-6225 Mass Termination Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the USB-6225 Mass Termination device. Refer to `ni.com` for other accessory options, including new devices.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SH68-68-EP shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. Connector 1 cannot be used with SCCs.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

Using a BNC Accessory with Connector 0

Connector 0 of your device is compatible with several BNC accessories:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use the SH68-68-EP shielded cable, to connect Connector 0 of your DAQ device to BNC accessories.

Using a BNC Accessory with Connector 1

Connector 1 of your device is compatible with BNC-2115. BNC-2115 provides BNC connectivity to 24 of the differential (48 single ended) analog input signals on Connector 1.

You can use an SH68-68-S cable to connect to the BNC-2115.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH68-68-EP shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor (make sure the switches are set properly)[1]
- TBX-68 DIN rail-mountable connector block

You can use one screw terminal accessory with the signals on either connector of your USB-6225 Mass Termination device. You can use two screw terminal accessories with one M Series device by using both connectors.[2]

Cables

Choosing a Cable for Connector 0

In most applications, you can use the following cables with Connector 0:

- **SH68-68-EP**—High-performance cable with individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **R68-68**—Highly-flexible unshielded ribbon cable

Choosing a Cable for Connector 1

In most applications, you can use the following cables with Connector 1:

- **SH68-68-S**—Shielded cable with 34 twisted pairs of wire. Each differential analog input channel on Connector 1 is routed on a twisted pair on the SH68-68-S cable
- **R68-68**—Highly flexible unshielded ribbon cable

[1] NI recommends that you use the SH68-68-S cable when the SCB-68 is connected to Connector 1.

[2] The SCC-68 only can be used with Connector 0.

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6225 Mass Termination LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6225 Mass Termination LEDs.

USB-6225 Mass Termination Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6225 Mass Termination.

NI 6229

The following sections contain information about the PCI/PXI-6229, USB-6229 Screw Terminal, and USB-6229 BNC devices.

PCI/PXI-6229

PCI/PXI-6229 Pinout

Figure A-17 shows the pinout of the PCI/PXI-6229. The I/O signals appear on two 68-pin connectors.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

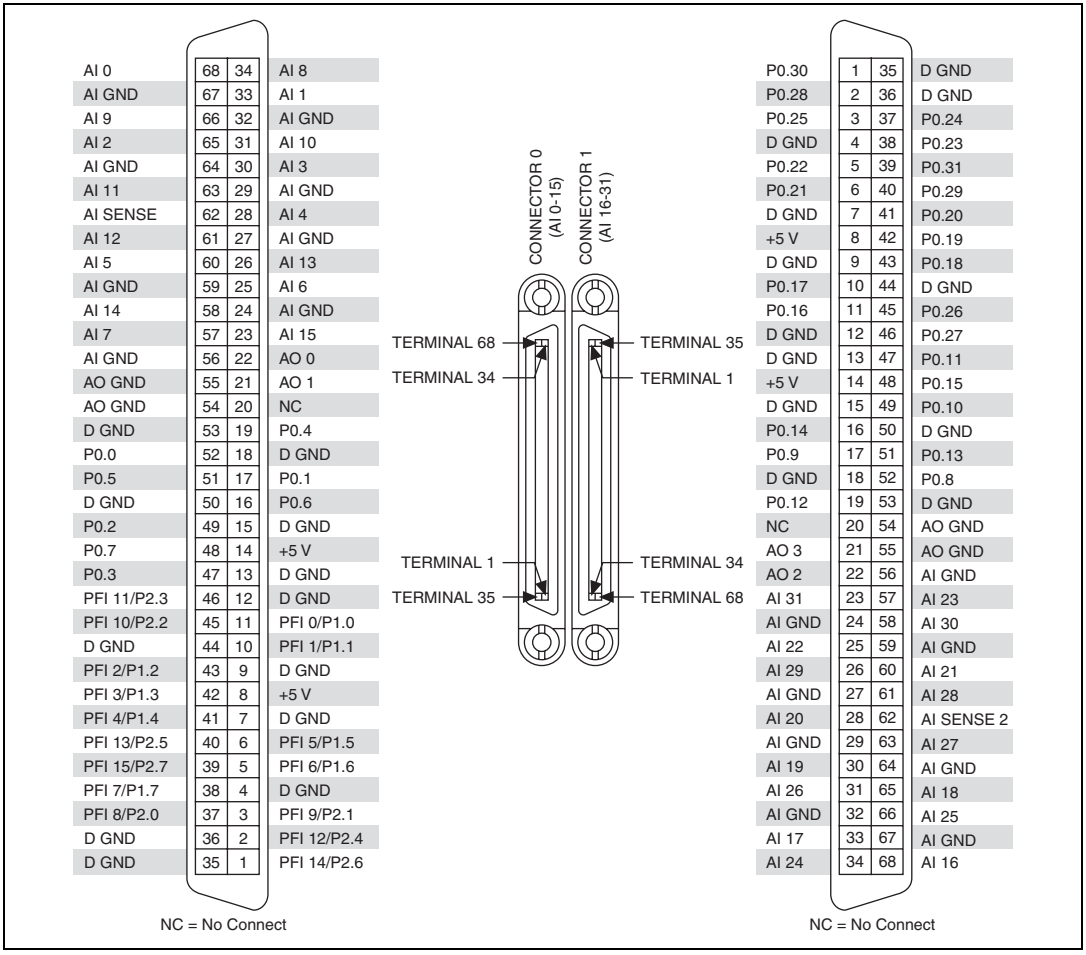

Figure A-17. PCI/PXI-6229 Pinout

Table A-10. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6229 Specifications

Refer to the *NI 622x Specifications* for more detailed information about the PCI/PXI-6229 device.

PCI/PXI-6229 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the PCI/PXI-6229. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. NI-DAQ 7.4 and later supports SCXI in parallel mode on Connector 1.

Note When using Connector 1 in parallel mode with SCXI modules that support track and hold, you must programmatically disable track and hold.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output

- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706[1] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

[1] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6229 Screw Terminal

USB-6229 Screw Terminal Pinout

Figure A-18 shows the pinout of the USB-6229 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

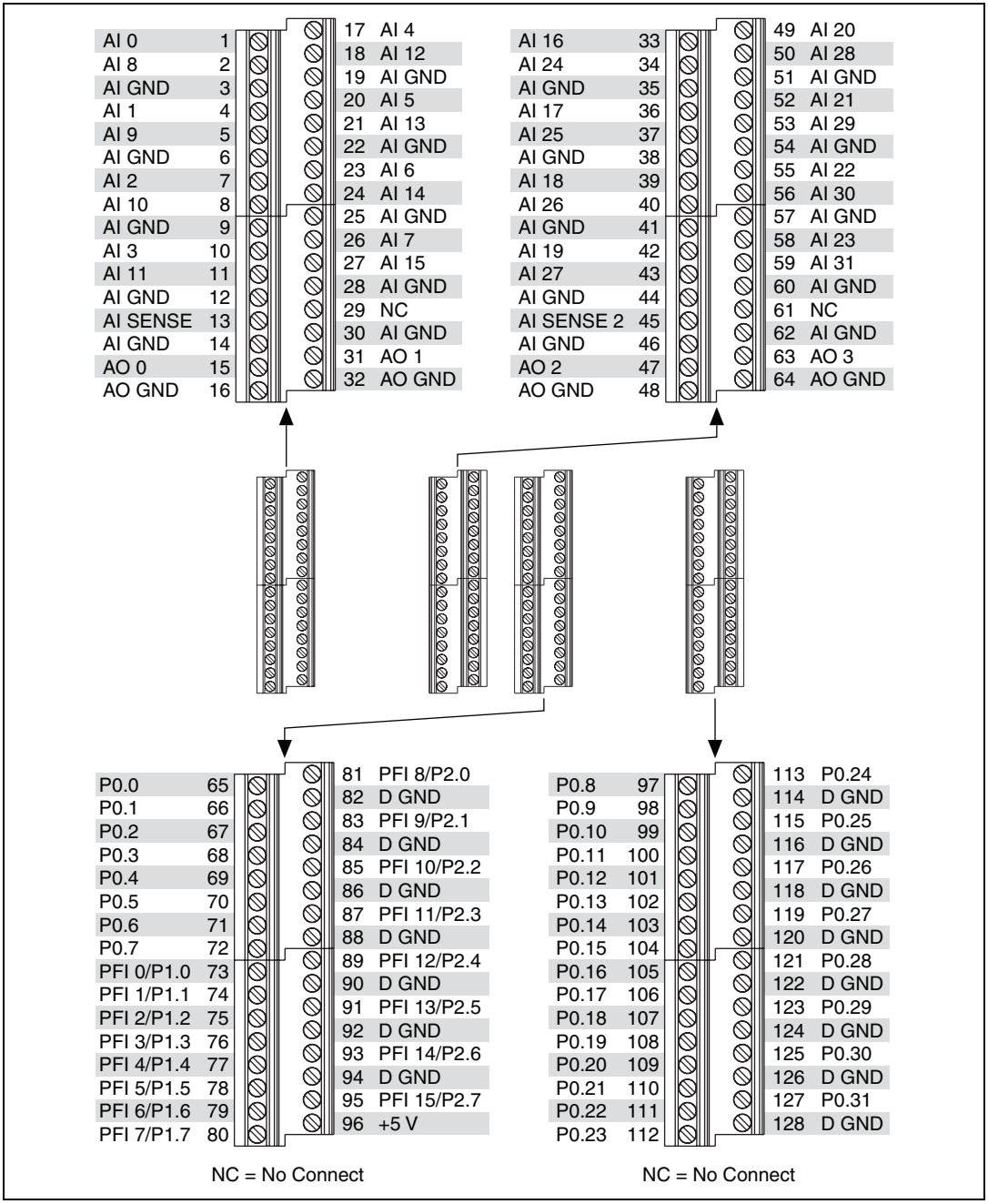

Figure A-18. USB-6229 Screw Terminal Pinout

Table A-11. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	81 (PFI 8)
CTR 0 GATE	83 (PFI 9)
CTR 0 AUX	85 (PFI 10)
CTR 0 OUT	89 (PFI 12)
CTR 0 A	81 (PFI 8)
CTR 0 Z	83 (PFI 9)
CTR 0 B	85 (PFI 10)
CTR 1 SRC	76 (PFI 3)
CTR 1 GATE	77 (PFI 4)
CTR 1 AUX	87 (PFI 11)
CTR 1 OUT	91 (PFI 13)
CTR 1 A	76 (PFI 3)
CTR 1 Z	77 (PFI 4)
CTR 1 B	87 (PFI 11)
FREQ OUT	93 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6229 Screw Terminal Specifications

Refer to the *NI 622x Specifications* for more detailed information about the USB-6229 Screw Terminal device.

USB-6229 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6229 Screw Terminal LEDs.

USB-6229 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6229 Screw Terminal.

USB-6229 BNC

USB-6229 BNC Pinout

Figure A-19 shows the pinout of the USB-6229 BNC.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

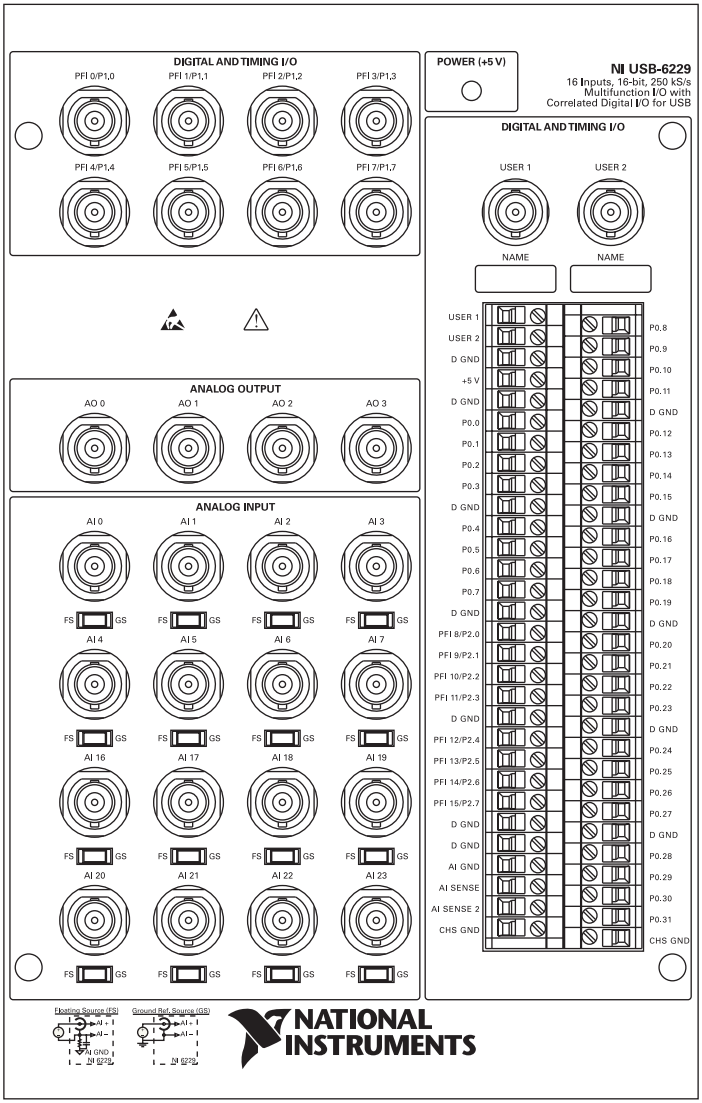

Figure A-19. USB-6229 BNC Top Panel and Pinout

Table A-12. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Name
CTR 0 SRC	PFI 8
CTR 0 GATE	PFI 9
CTR 0 AUX	PFI 10
CTR 0 OUT	PFI 12
CTR 0 A	PFI 8
CTR 0 Z	PFI 9
CTR 0 B	PFI 10
CTR 1 SRC	PFI 3
CTR 1 GATE	PFI 4
CTR 1 AUX	PFI 11
CTR 1 OUT	PFI 13
CTR 1 A	PFI 3
CTR 1 Z	PFI 4
CTR 1 B	PFI 11
FREQ OUT	PFI 14

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Connecting Signals to the USB-6229 BNC

Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

Differential Signals

To connect differential signals, determine the type of signal source you are using—a floating signal (FS) source or a ground-referenced signal (GS) source. Refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*, for more information.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-20 shows the AI 0 BNC and corresponding FS/GS switch on the top panel of the USB-6229 BNC.

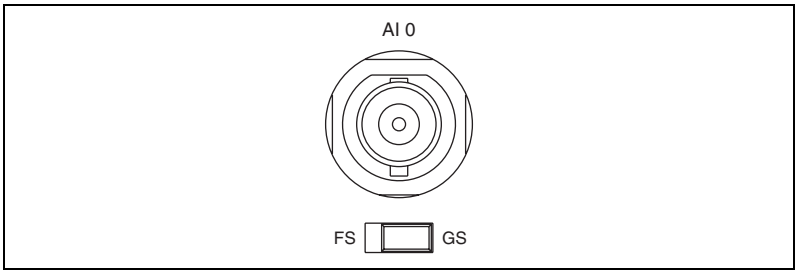

Figure A-20. FS/GS Switch

Figure A-21 shows the analog input circuitry on the USB-6229 BNC. When the switch is set to the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

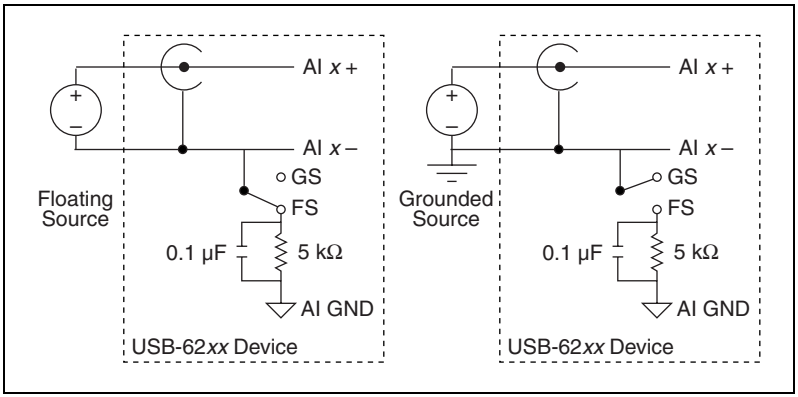

Figure A-21. Analog Input Circuitry

Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-22.

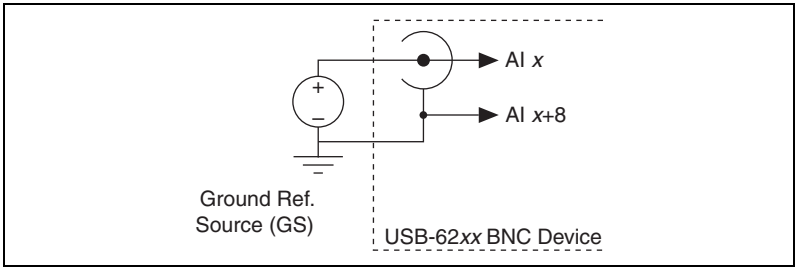

Figure A-22. Single-Ended Channels

When you set the source type to the GS position and configure the device for single-ended input in software, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 32 single-ended channels are available in single-ended measurement modes.

For information on how to connect your single-ended signals, AI GND, and/or AI SENSE, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*. For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-23 shows the analog output circuitry on the USB-6229 BNC.

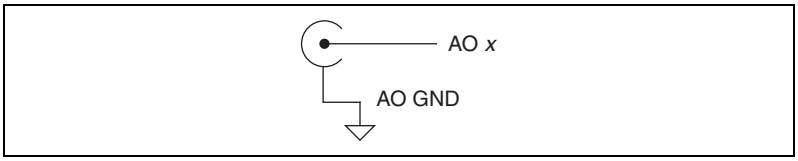

Figure A-23. Analog Output Circuitry

Refer to the *Connecting Analog Output Signals* section of Chapter 5, *Analog Output*, for more information.

Digital I/O and Timing I/O

You can access digital I/O and timing I/O signals on the BNC connectors labeled PFI <0..7>/P1.<0..7>. Figure A-24 shows the DIO/TIO circuitry on the USB-6229 BNC.

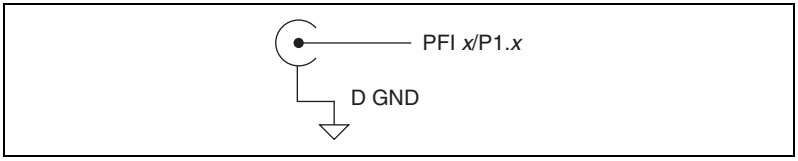

Figure A-24. Digital I/O and Timing I/O Circuitry

Refer to the *Connecting Digital I/O Signals* section of Chapter 6, *Digital I/O*, and the *Connecting PFI Input Signals* section of Chapter 8, *PFI*, for more information.

USER 1 and USER 2

The USER 1 and USER 2 BNC connectors allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 and USER 2 BNC connectors are routed (internal to the USB-6229 BNC) to the USER 1 and USER 2 screw terminals, as shown in Figure A-25.

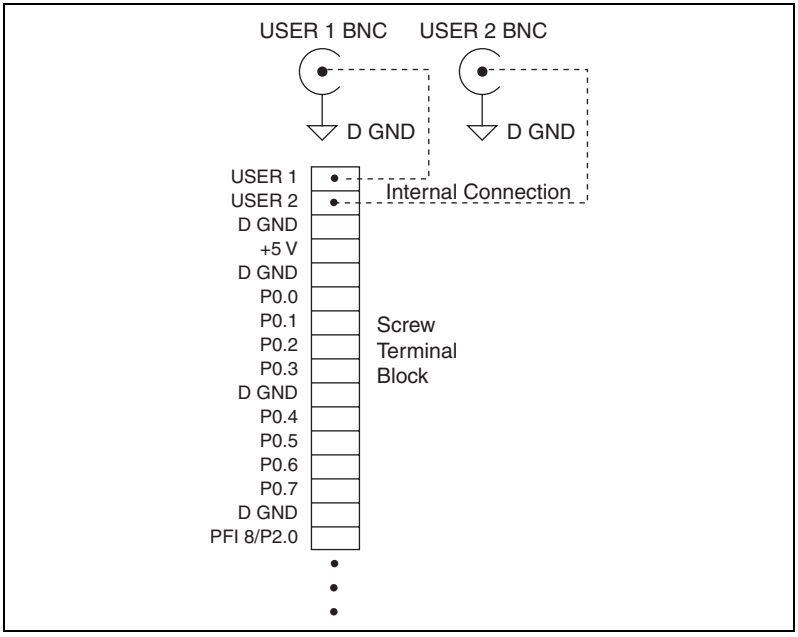

Figure A-25. USER 1 and USER 2 BNC Connections

Figure A-26 shows an example of how to use the USER 1 and USER 2 BNCs. To access the PFI 8 signal from a BNC, connect USER 1 on the screw terminal block to PFI 8 with a wire.

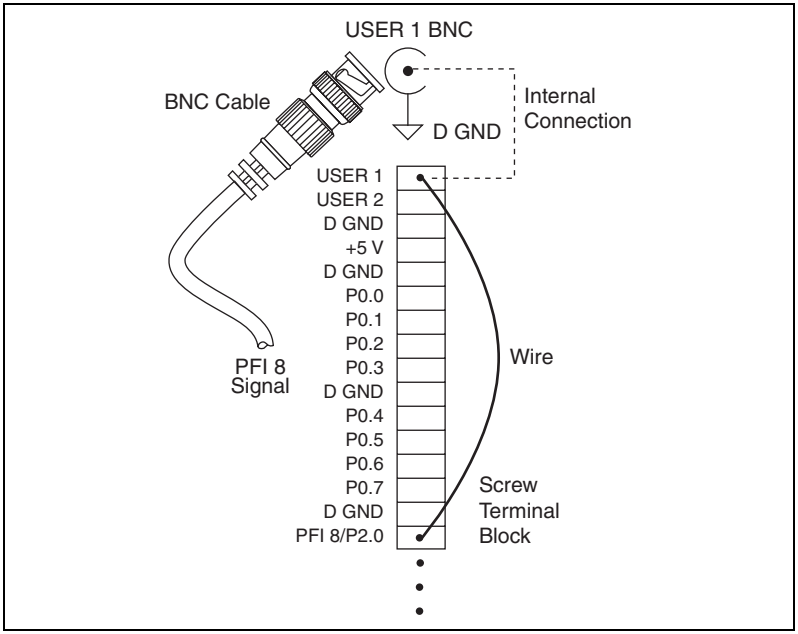

Figure A-26. Connecting PFI 8 to USER 1 BNC

The designated space below each USER <1..2> BNC is for marking or labeling signal names.

USB-6229 BNC Specifications

Refer to the *NI 622x Specifications* for more detailed information about the USB-6229 BNC device.

USB-6229 BNC LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6229 BNC LEDs.

USB-6229 BNC Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6229 BNC.

NI 6250

PCI/PXI-6250 Pinout

Figure A-27 shows the pinout of the PCI/PXI-6250.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

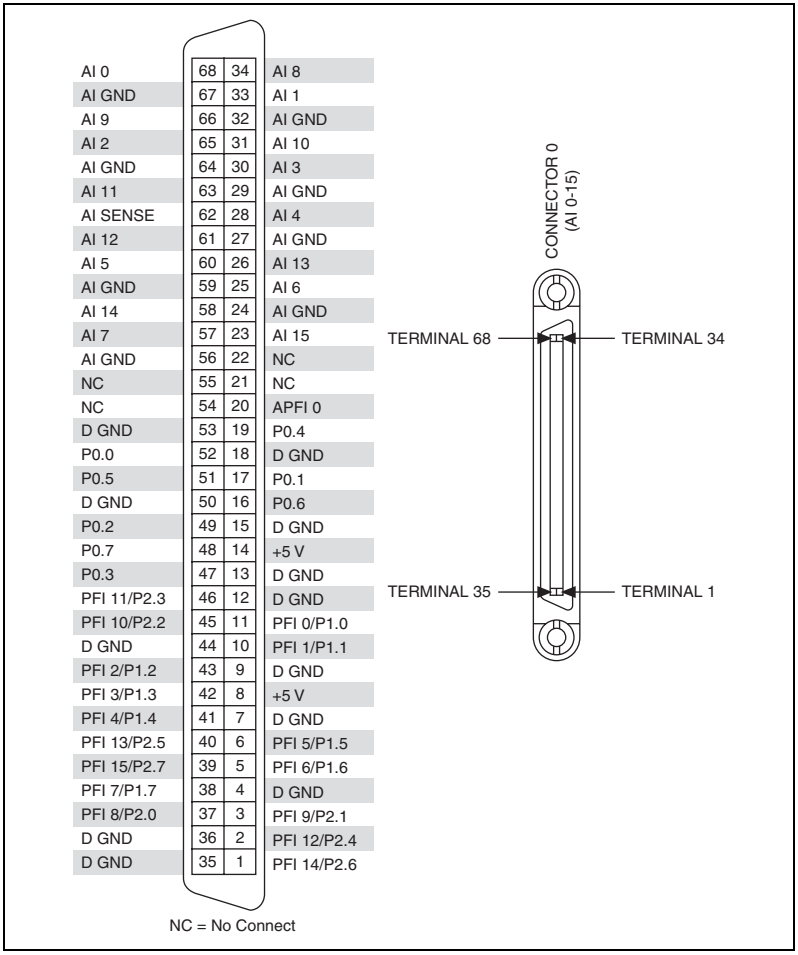

Figure A-27. PCI/PXI-6250 Pinout

Table A-13. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6250 Specifications

Refer to the *NI 625x Specifications* for more detailed information about the PCI/PXI-6250 device.

PCI/PXI-6250 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the PCI/PXI-6250. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706 front panel mounted terminal block for PXI M Series devices

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

NI 6251

The following sections contain information about the NI PCI/PCIe/PXI/PXIe-6251, USB-6251 Screw Terminal, USB-6251 BNC, and USB-6251 Mass Termination devices.

NI PCI/PCIe/PXI/PXIe-6251

NI PCI/PCIe/PXI/PXIe-6251 Pinout

Figure A-28 shows the pinout of the NI PCI/PCIe/PXI/PXIe-6251.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

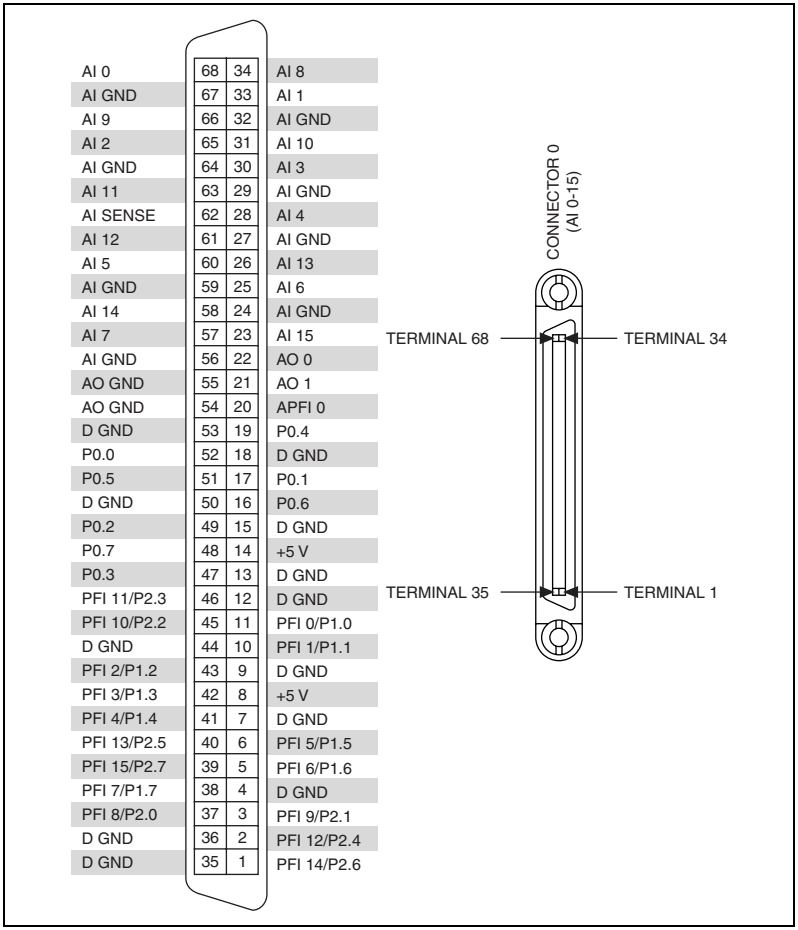

Figure A-28. NI PCI/PCIe/PXI/PXIe-6251 Pinout

Table A-14. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

NI PCI/PCIe/PXI/PXIe-6251 Specifications

Refer to the *NI 625x Specifications* for more detailed information about the NI PCI/PCIe/PXI/PXIe-6251 device.

NI PCI/PCIe/PXI/PXIe-6251 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the NI PCI/PCIe/PXI/PXIe-6251. Refer to `ni.com` for other accessory options including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Note PCI Express users should consider the power limits on certain SCC modules without an external power supply. Refer to the *NI 625x Specifications*, and the *Disk Drive Power Connector* section of Chapter 3, *Connector and LED Information*, for information about power limits and increasing the current the device can supply on the +5 V terminal.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
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- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
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- TB-2706 front panel mounted terminal block for PXI M Series devices

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Use RTSI bus cables to connect timing and synchronization signals among PCI/PCI Express devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
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Custom Cabling and Connectivity

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Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6251 Screw Terminal

USB-6251 Screw Terminal Pinout

Figure A-29 shows the pinout of the USB-6251 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

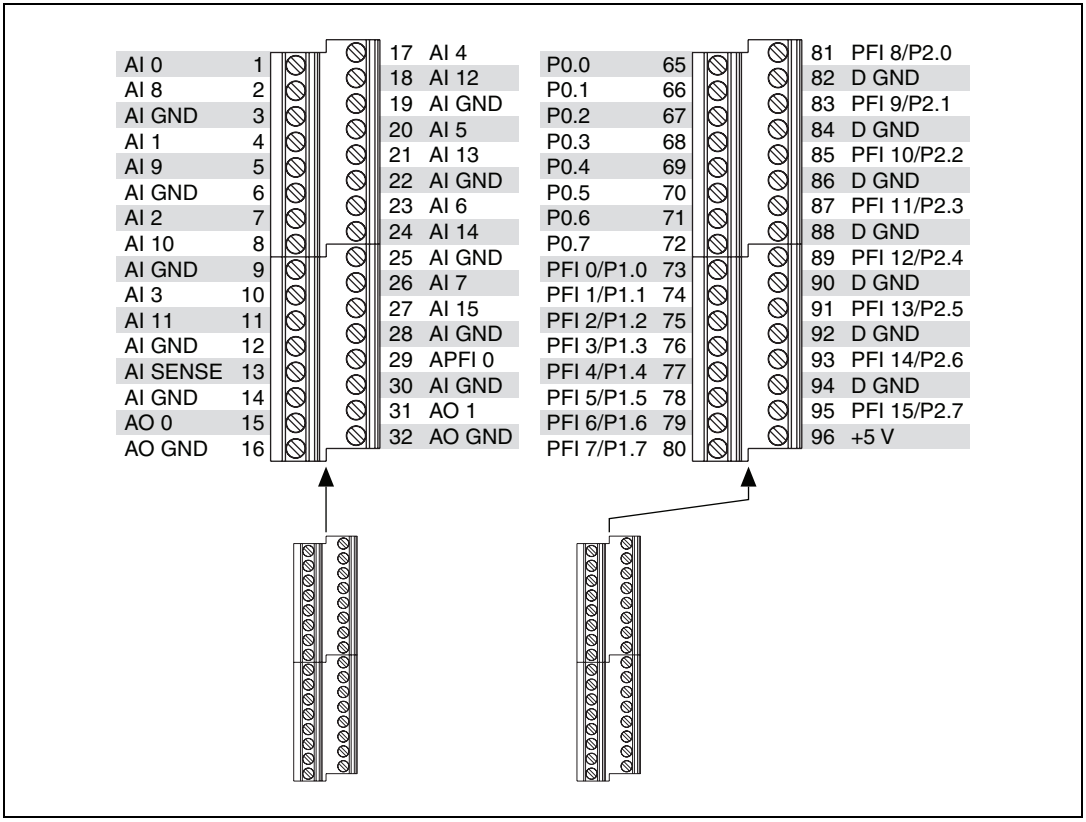

Figure A-29. USB-6251 Screw Terminal Pinout

Table A-15. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	81 (PFI 8)
CTR 0 GATE	83 (PFI 9)
CTR 0 AUX	85 (PFI 10)
CTR 0 OUT	89 (PFI 12)
CTR 0 A	81 (PFI 8)
CTR 0 Z	83 (PFI 9)
CTR 0 B	85 (PFI 10)
CTR 1 SRC	76 (PFI 3)
CTR 1 GATE	77 (PFI 4)
CTR 1 AUX	87 (PFI 11)
CTR 1 OUT	91 (PFI 13)
CTR 1 A	76 (PFI 3)
CTR 1 Z	77 (PFI 4)
CTR 1 B	87 (PFI 11)
FREQ OUT	93 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6251 Screw Terminal Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6251 Screw Terminal device.

USB-6251 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6251 Screw Terminal LEDs.

USB-6251 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6251 Screw Terminal.

USB-6251 BNC

USB-6251 BNC Pinout

Figure A-30 shows the pinout of the USB-6251 BNC.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

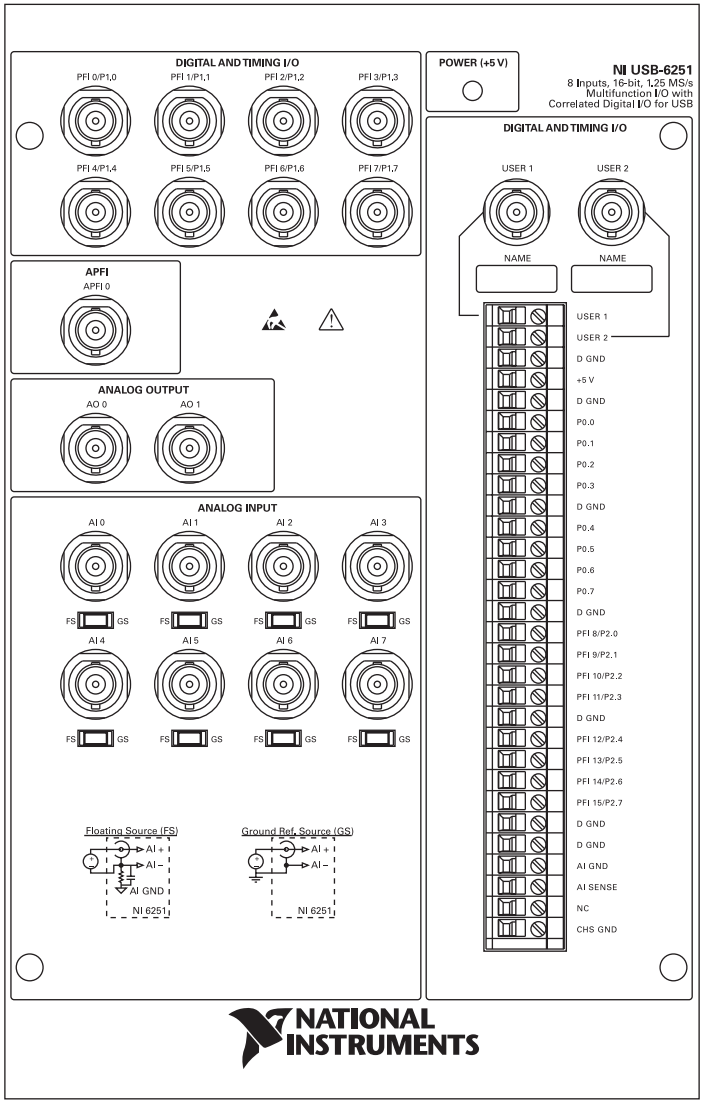

Figure A-30. USB-6251 BNC Top Panel and Pinout

Table A-16. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Name
CTR 0 SRC	PFI 8
CTR 0 GATE	PFI 9
CTR 0 AUX	PFI 10
CTR 0 OUT	PFI 12
CTR 0 A	PFI 8
CTR 0 Z	PFI 9
CTR 0 B	PFI 10
CTR 1 SRC	PFI 3
CTR 1 GATE	PFI 4
CTR 1 AUX	PFI 11
CTR 1 OUT	PFI 13
CTR 1 A	PFI 3
CTR 1 Z	PFI 4
CTR 1 B	PFI 11
FREQ OUT	PFI 14

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Connecting Signals to the USB-6251 BNC

Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

Differential Signals

To connect differential signals, determine the type of signal source you are using—a floating signal (FS) source or a ground-referenced signal (GS) source. Refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*, for more information.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-31 shows the AI 0 BNC and corresponding FS/GS switch on the top panel of the USB-6251 BNC.

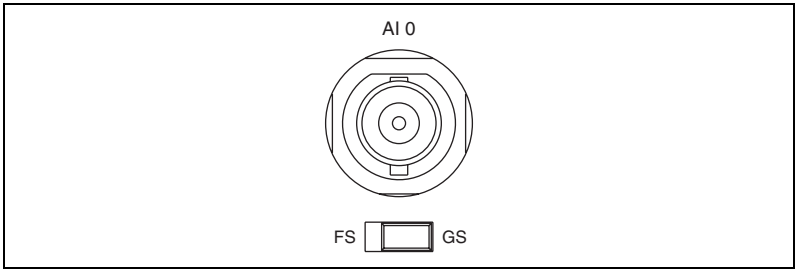

Figure A-31. FS/GS Switch

Figure A-32 shows the analog input circuitry on the USB-6251 BNC. When the switch is set to the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

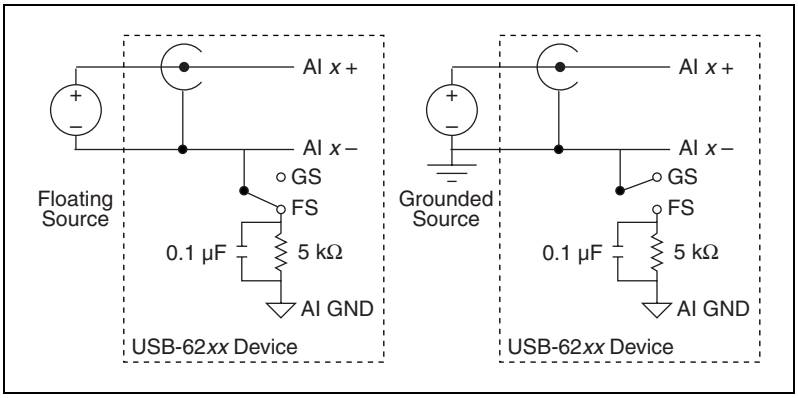

Figure A-32. Analog Input Circuitry

Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-33.

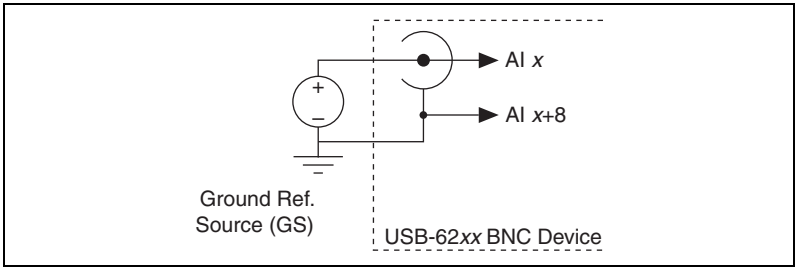

Figure A-33. Single-Ended Channels

When you set the source type to the GS position and configure the device for single-ended input in software, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 16 single-ended channels are available in single-ended measurement modes.

For information on how to connect your single-ended signals, AI GND, and/or AI SENSE, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*. For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-34 shows the analog output circuitry on the USB-6251 BNC.

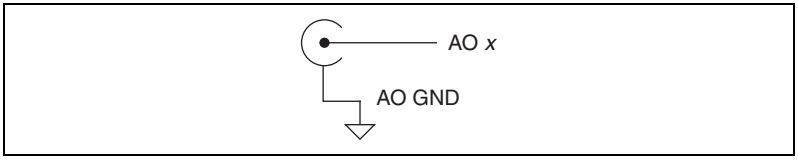

Figure A-34. Analog Output Circuitry

Refer to the *Connecting Analog Output Signals* section of Chapter 5, *Analog Output*, for more information.

Digital I/O and Timing I/O

You can access digital I/O and timing I/O signals on the BNC connectors labeled PFI <0..7>/P1.<0..7>. Figure A-35 shows the DIO/TIO circuitry on the USB-6251 BNC.

Figure A-35. Digital I/O and Timing I/O Circuitry

Refer to the *Connecting Digital I/O Signals* section of Chapter 6, *Digital I/O*, and the *Connecting PFI Input Signals* section of Chapter 8, *PFI*, for more information.

APFI

You can access the analog programmable function interface signal on the BNC connector labeled APFI 0. Figure A-36 shows the APFI circuitry on the USB-6251 BNC.

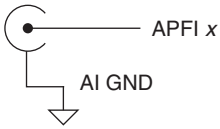

Figure A-36. Analog Programmable Function Interface Circuitry

Refer to the *Triggering with an Analog Source* section of Chapter 11, *Triggering*, for more information.

USER 1 and USER 2

The USER 1 and USER 2 BNC connectors allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 and USER 2 BNC connectors are routed (internal to the USB-6251 BNC) to the USER 1 and USER 2 screw terminals, as shown in Figure A-37.

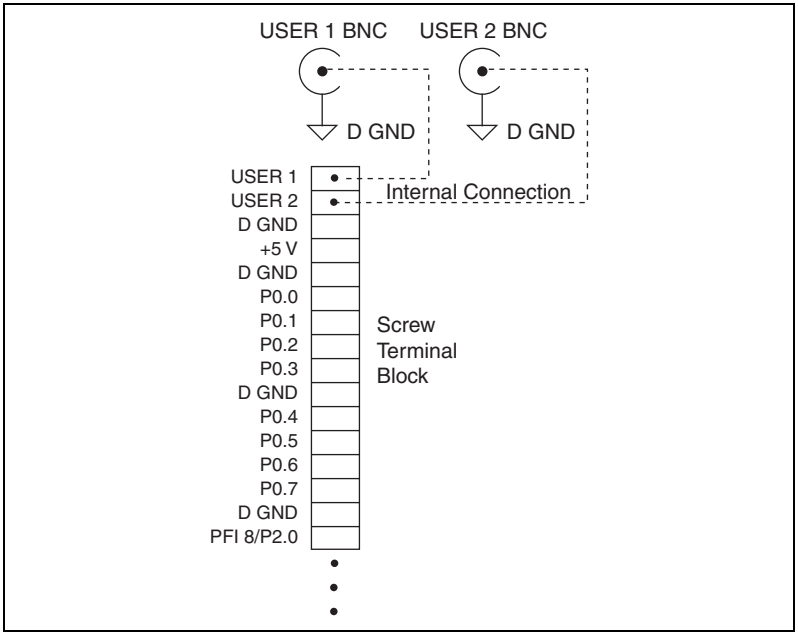

Figure A-37. USER 1 and USER 2 BNC Connections

Figure A-38 shows an example of how to use the USER 1 and USER 2 BNCs. To access the PFI 8 signal from a BNC, connect USER 1 on the screw terminal block to PFI 8 with a wire.

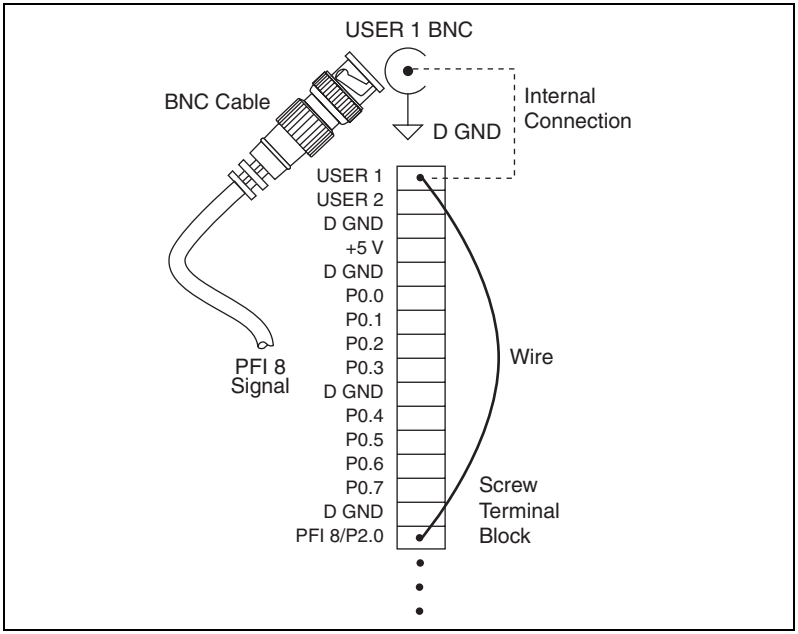

Figure A-38. Connecting PFI 8 to USER 1 BNC

The designated space below each USER <1..2> BNC is for marking or labeling signal names.

USB-6251 BNC Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6251 BNC device.

USB-6251 BNC LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6251 BNC LEDs.

USB-6251 BNC Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6251 BNC.

USB-6251 Mass Termination

USB-6251 Mass Termination Pinout

Figure A-39 shows the pinout of the USB-6251 Mass Termination device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

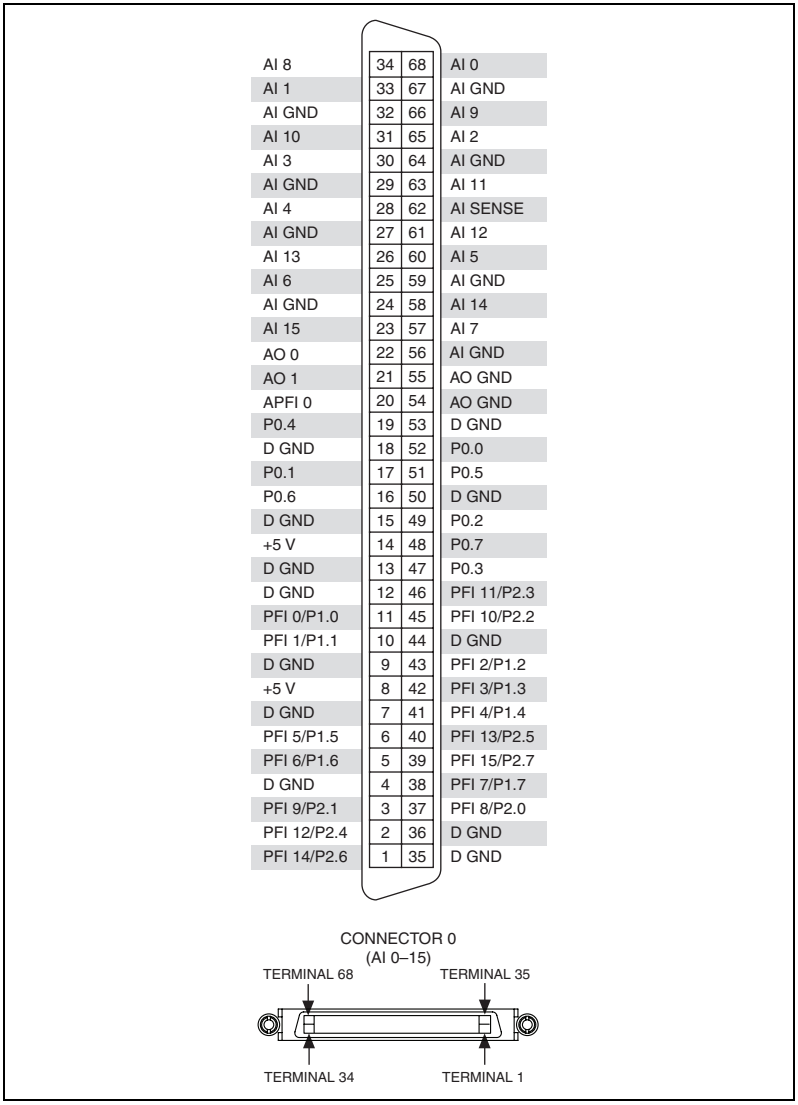

Figure A-39. USB-6251 Mass Termination Pinout

Table A-17. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6251 Mass Termination Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6251 Mass Termination device.

USB-6251 Mass Termination Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the USB-6251 Mass Termination device. Refer to `ni.com` for other accessory options, including new devices.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SH68-68-EP shielded cable.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SH68-68-EP shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH68-68-EP shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
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- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block

Cables

In most applications, you can use the following cables:

- **SH68-68-EP**—High-performance cable with individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
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The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6251 Mass Termination LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6251 Mass Termination LEDs.

USB-6251 Mass Termination Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6251 Mass Termination.

NI 6254

PCI/PXI-6254 Pinout

Figure A-40 shows the pinout of the PCI/PXI-6254. The I/O signals appear on two 68-pin connectors.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

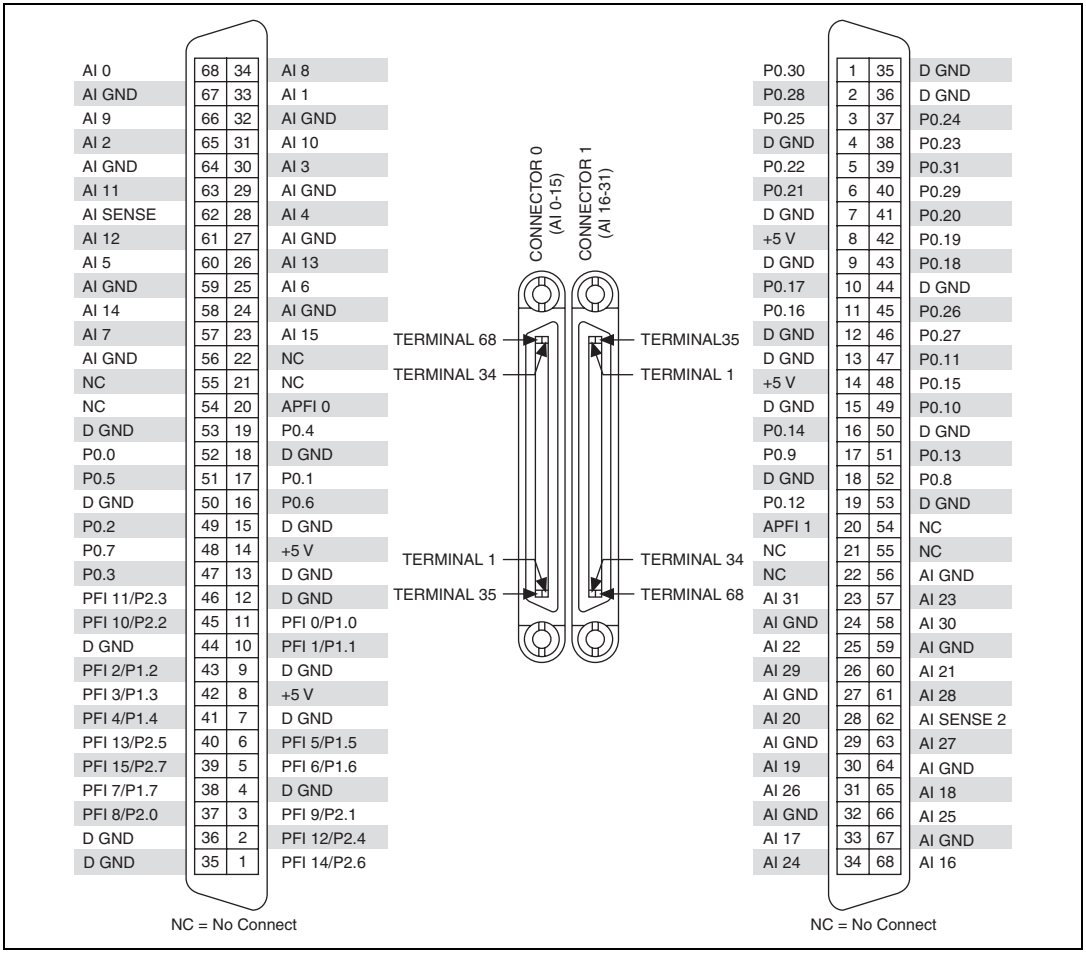

Figure A-40. PCI/PXI-6254 Pinout

Table A-18. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6254 Specifications

Refer to the *NI 625x Specifications* for more detailed information about the PCI/PXI-6254 device.

PCI/PXI-6254 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the PCI/PXI-6254. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. NI-DAQ 7.4 and later supports SCXI in parallel mode on Connector 1.

Note When using Connector 1 in parallel mode with SCXI modules that support track and hold, you must programmatically disable track and hold.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706[1] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

[1] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

NI 6255

The following sections contain information about the PCI/PXI-6255, USB-6255 Screw Terminal, and USB-6255 Mass Termination devices.

PCI/PXI-6255

PCI/PXI-6255 Pinout

Figure A-41 shows the pinout of the PCI/PXI-6255.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

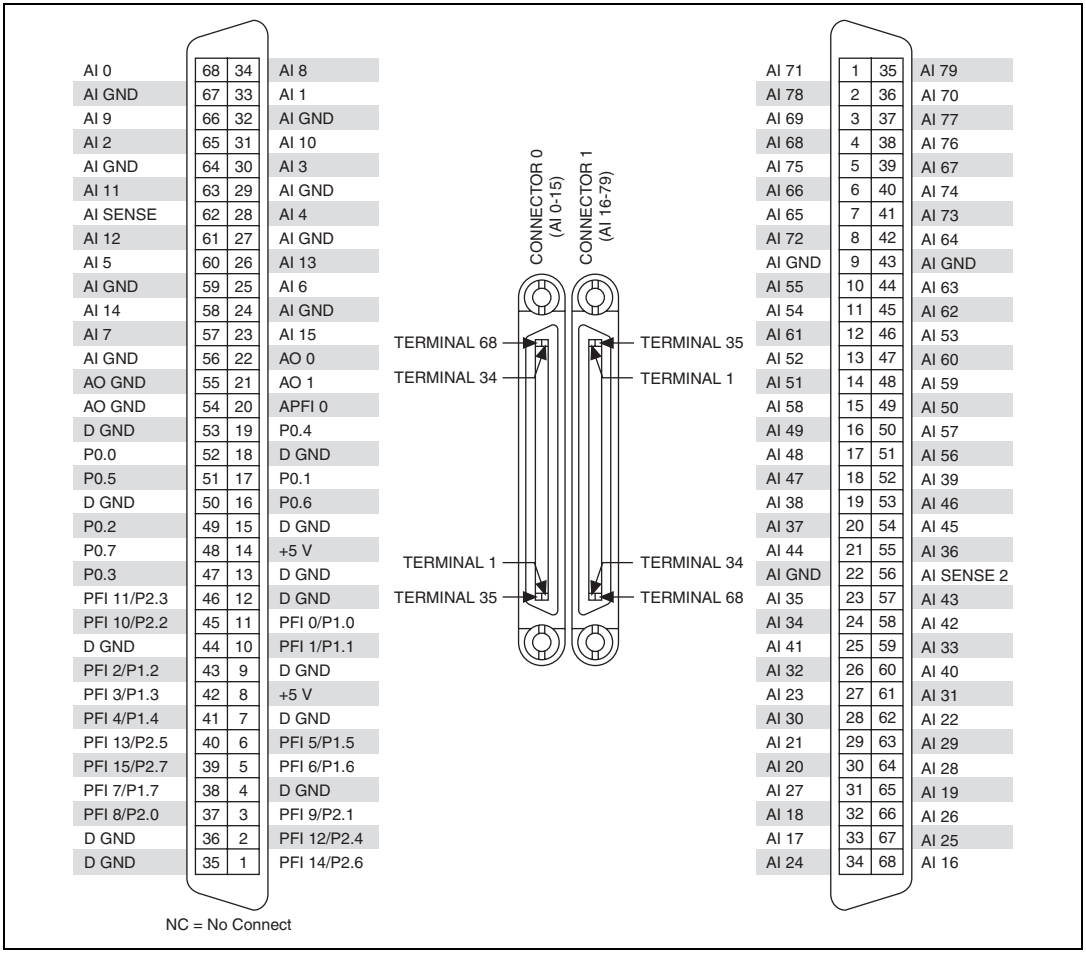

Figure A-41. PCI/PXI-6255 Pinout

Table A-19. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6255 Specifications

Refer to the *NI 625x Specifications* for more detailed information about the PCI/PXI-6255 device.

PCI/PXI-6255 Accessory and Cabling Options

This section describes some cable and accessory options for the PCI/PXI-6255. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. Connector 1 cannot be used to control SCXI.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. Connector 1 cannot be used with SCCs.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

Using a BNC Accessory with Connector 0

Connector 0 of your device is compatible with several BNC accessories:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use the SHC68-68-EPM shielded cable, to connect Connector 0 of your DAQ device to BNC accessories.

Using a BNC Accessory with Connector 1

Connector 1 of your device is compatible with BNC-2115. BNC-2115 provides BNC connectivity to 24 of the differential (48 single ended) analog input signals on Connector 1.

You can use an SHC68-68 cable to connect to the BNC-2115.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks such as:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor (make sure the switches are set properly)[1]
- TBX-68 DIN rail-mountable connector block
- TB-2706[2] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.[3]

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

The PCI/PXI-6255 has two connectors that require different cables.

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[1] NI recommends that you use the SHC68-68 cable when the SCB-68 is connected to Connector 1.

[2] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

[3] The SCC-68 only can be used with Connector 0.

Choosing a Cable for Connector 0

In most applications, you can use the following cables with Connector 0:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Choosing a Cable for Connector 1

In most applications, you can use the following cables with Connector 1:

- **SHC68-68**—Shielded cable with 34 twisted pairs of wire. Each differential analog input channel on Connector 1 is routed on a twisted pair on the SHC68-68 cable
- **RC68-68**—Highly flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6255 Screw Terminal

USB-6255 Screw Terminal Pinout

Figure A-42 shows the pinout of the USB-6255 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note For a ground connection, you can connect the shield of a shielded cable to the chassis ground lug, depicted in Figure A-42.

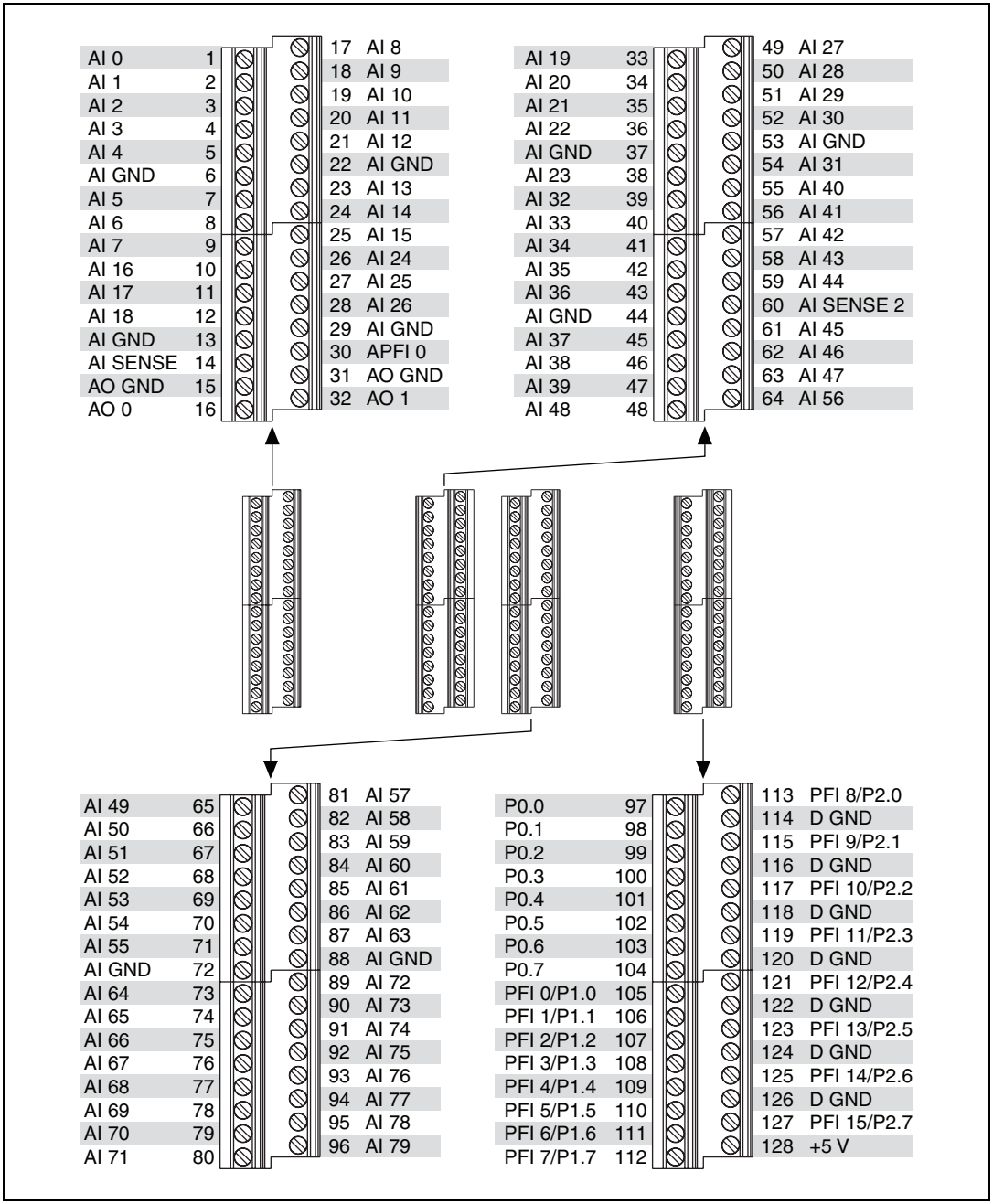

Figure A-42. USB-6255 Screw Terminal Pinout

Table A-20. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	113 (PFI 8)
CTR 0 GATE	115 (PFI 9)
CTR 0 AUX	117 (PFI 10)
CTR 0 OUT	121 (PFI 12)
CTR 0 A	113 (PFI 8)
CTR 0 Z	115 (PFI 9)
CTR 0 B	117 (PFI 10)
CTR 1 SRC	108 (PFI 3)
CTR 1 GATE	109 (PFI 4)
CTR 1 AUX	119 (PFI 11)
CTR 1 OUT	123 (PFI 13)
CTR 1 A	108 (PFI 3)
CTR 1 Z	109 (PFI 4)
CTR 1 B	119 (PFI 11)
FREQ OUT	125 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6255 Screw Terminal Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6255 Screw Terminal device.

USB-6255 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6255 Screw Terminal LEDs.

USB-6255 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6255 Screw Terminal.

USB-6255 Mass Termination

USB-6255 Mass Termination Pinout

Figure A-43 shows the pinout of the USB-6255 Mass Termination device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

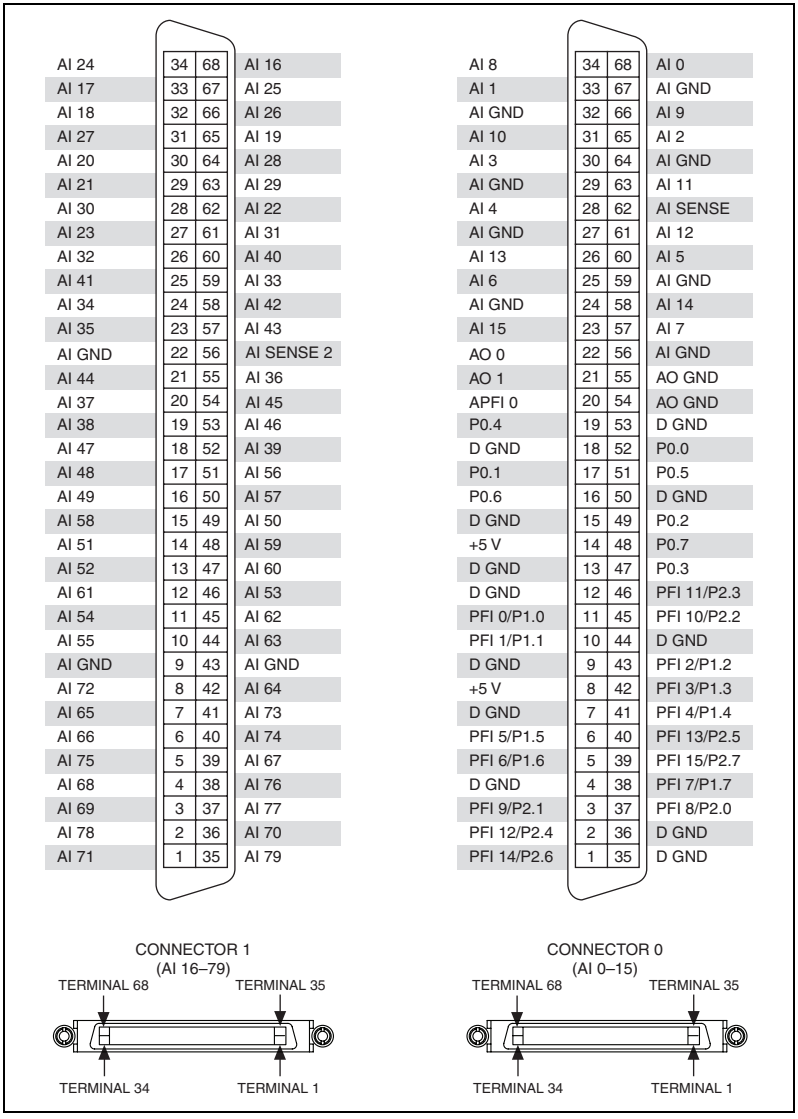

Figure A-43. USB-6255 Mass Termination Pinout

Table A-21. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6255 Mass Termination Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6255 Mass Termination device.

USB-6255 Mass Termination Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the USB-6255 Mass Termination device. Refer to `ni.com` for other accessory options, including new devices.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SH68-68-EP shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. Connector 1 cannot be used with SCCs.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

Using a BNC Accessory with Connector 0

Connector 0 of your device is compatible with several BNC accessories:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use the SH68-68-EP shielded cable, to connect Connector 0 of your DAQ device to BNC accessories.

Using a BNC Accessory with Connector 1

Connector 1 of your device is compatible with BNC-2115. BNC-2115 provides BNC connectivity to 24 of the differential (48 single ended) analog input signals on Connector 1.

You can use an SH68-68-S cable to connect to the BNC-2115.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH68-68-EP shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor (make sure the switches are set properly)[1]
- TBX-68 DIN rail-mountable connector block

You can use one screw terminal accessory with the signals on either connector of your USB-6255 Mass Termination device. You can use two screw terminal accessories with one M Series device by using both connectors.[2]

Cables

Choosing a Cable for Connector 0

In most applications, you can use the following cables with Connector 0:

- **SH68-68-EP**—High-performance cable with individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **R68-68**—Highly-flexible unshielded ribbon cable

Choosing a Cable for Connector 1

In most applications, you can use the following cables with Connector 1:

- **SH68-68-S**—Shielded cable with 34 twisted pairs of wire. Each differential analog input channel on Connector 1 is routed on a twisted pair on the SH68-68-S cable
- **R68-68**—Highly flexible unshielded ribbon cable

[1] NI recommends that you use the SH68-68-S cable when the SCB-68 is connected to Connector 1.

[2] The SCC-68 only can be used with Connector 0.

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6255 Mass Termination LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6255 Mass Termination LEDs.

USB-6255 Mass Termination Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6255 Mass Termination.

NI 6259

The following sections contain information about the NI PCI/PCIe/PXI/PXIe-6259, USB-6259 Screw Terminal, USB-6259 BNC, and USB-6259 Mass Termination devices.

NI PCI/PCIe/PXI/PXIe-6259

NI PCI/PCIe/PXI/PXIe-6259 Pinout

Figure A-44 shows the pinout of the NI PCI/PCIe/PXI/PXIe-6259. The I/O signals appear on two 68-pin connectors.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

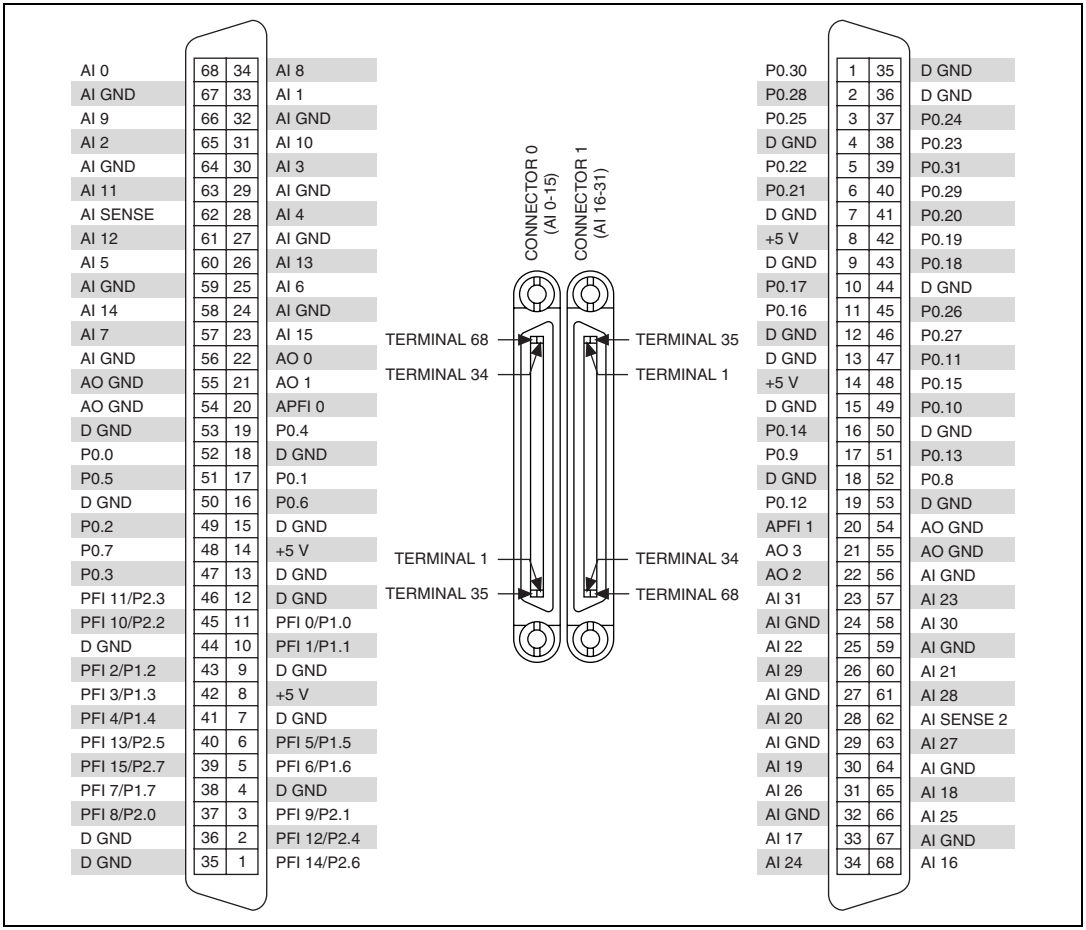

Figure A-44. NI PCI/PCIe/PXI/PXIe-6259 Pinout

Table A-22. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

NI PCI/PCIe/PXI/PXIe-6259 Specifications

Refer to the *NI 625x Specifications* for more detailed information about the NI PCI/PCIe/PXI/PXIe-6259 device.

NI PCI/PCIe/PXI/PXIe-6259 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the NI PCI/PCIe/PXI/PXIe-6259. Refer to `ni.com` for other accessory options including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. NI-DAQ 7.4 and later supports SCXI in parallel mode on Connector 1.

Note When using Connector 1 in parallel mode with SCXI modules that support track and hold, you must programmatically disable track and hold.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Note PCI Express users should consider the power limits on certain SCC modules without an external power supply. Refer to the *NI 625x Specifications*, and the *Disk Drive Power Connector* section of Chapter 3, *Connector and LED Information*, for information about power limits and increasing the current the device can supply on the +5 V terminal.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706[1] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

[1] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI/PCI Express devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6259 Screw Terminal

USB-6259 Screw Terminal Pinout

Figure A-45 shows the pinout of the USB-6259 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

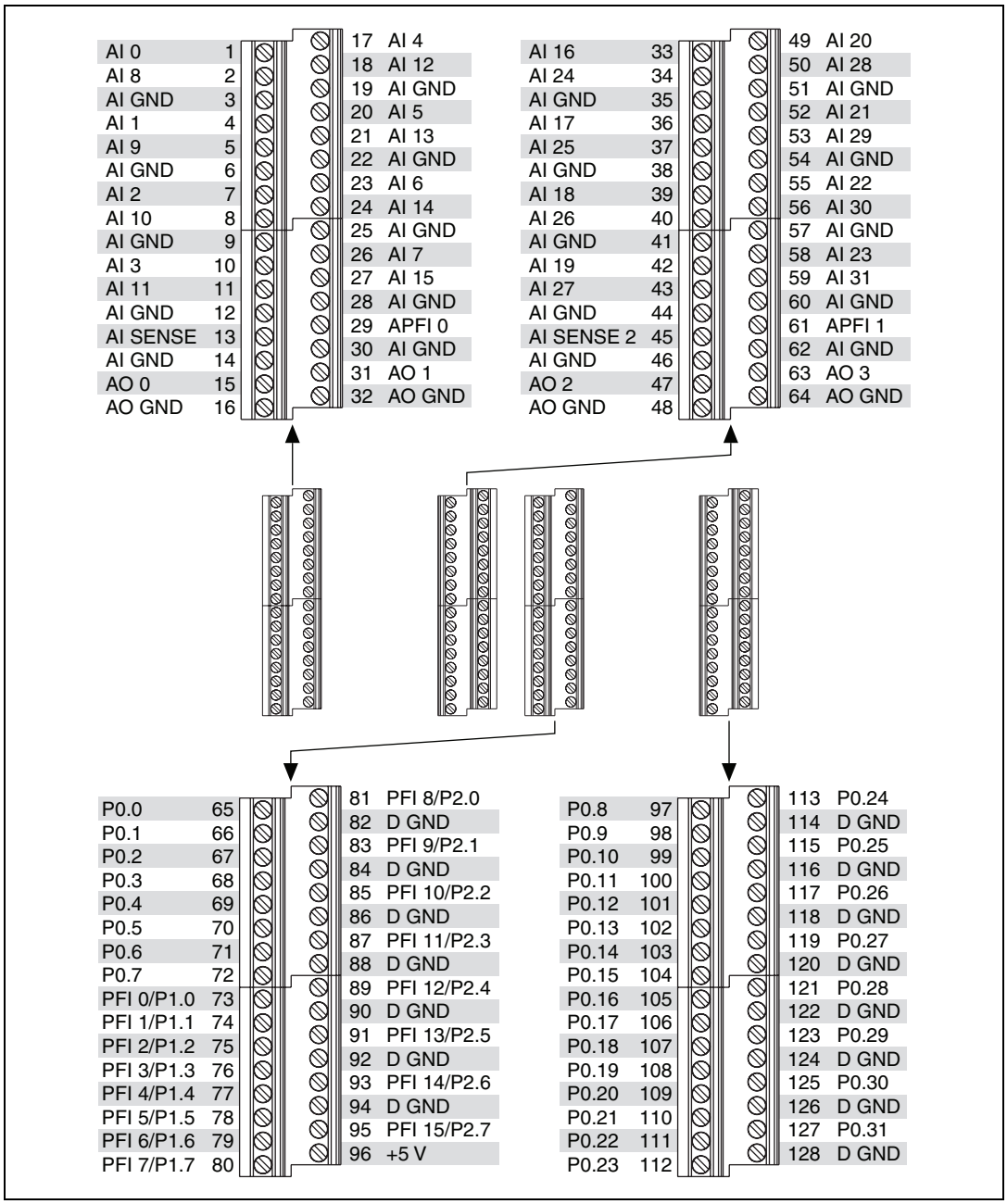

Figure A-45. USB-6259 Screw Terminal Pinout

Table A-23. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	81 (PFI 8)
CTR 0 GATE	83 (PFI 9)
CTR 0 AUX	85 (PFI 10)
CTR 0 OUT	89 (PFI 12)
CTR 0 A	81 (PFI 8)
CTR 0 Z	83 (PFI 9)
CTR 0 B	85 (PFI 10)
CTR 1 SRC	76 (PFI 3)
CTR 1 GATE	77 (PFI 4)
CTR 1 AUX	87 (PFI 11)
CTR 1 OUT	91 (PFI 13)
CTR 1 A	76 (PFI 3)
CTR 1 Z	77 (PFI 4)
CTR 1 B	87 (PFI 11)
FREQ OUT	93 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6259 Screw Terminal Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6259 Screw Terminal device.

USB-6259 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6259 Screw Terminal LEDs.

USB-6259 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6259 Screw Terminal.

USB-6259 BNC

USB-6259 BNC Pinout

Figure A-46 shows the pinout of the USB-6259 BNC.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

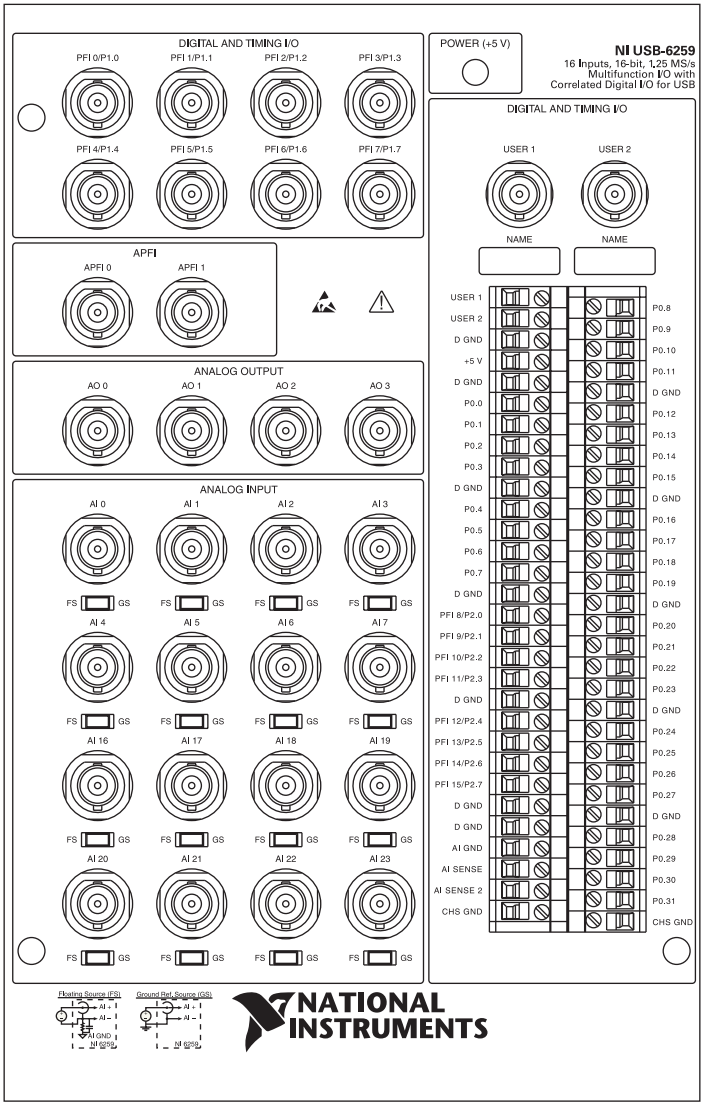

Figure A-46. USB-6259 BNC Top Panel and Pinout

Table A-24. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Name
CTR 0 SRC	PFI 8
CTR 0 GATE	PFI 9
CTR 0 AUX	PFI 10
CTR 0 OUT	PFI 12
CTR 0 A	PFI 8
CTR 0 Z	PFI 9
CTR 0 B	PFI 10
CTR 1 SRC	PFI 3
CTR 1 GATE	PFI 4
CTR 1 AUX	PFI 11
CTR 1 OUT	PFI 13
CTR 1 A	PFI 3
CTR 1 Z	PFI 4
CTR 1 B	PFI 11
FREQ OUT	PFI 14

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

Connecting Signals to the USB-6259 BNC

Analog Input

You can use each analog input BNC connector for one differential signal or two single-ended signals.

Differential Signals

To connect differential signals, determine the type of signal source you are using—a floating signal (FS) source or a ground-referenced signal (GS) source. Refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*, for more information.

To measure a floating signal source, move the switch to the FS position. To measure a ground-referenced signal source, move the switch to the GS position. Figure A-47 shows the AI 0 BNC and corresponding FS/GS switch on the top panel of the USB-6259 BNC.

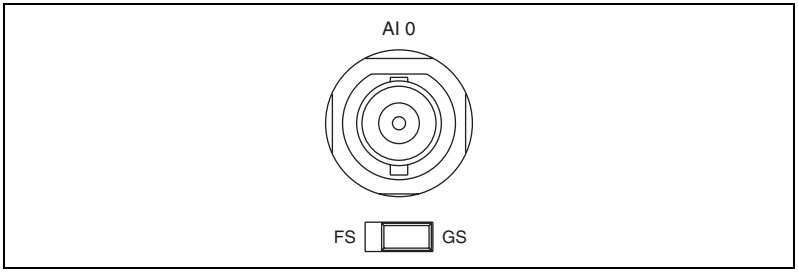

Figure A-47. FS/GS Switch

Figure A-48 shows the analog input circuitry on the USB-6259 BNC. When the switch is set to the FS position, AI *x* – is grounded through a 0.1 µF capacitor in parallel with a 5 kΩ resistor.

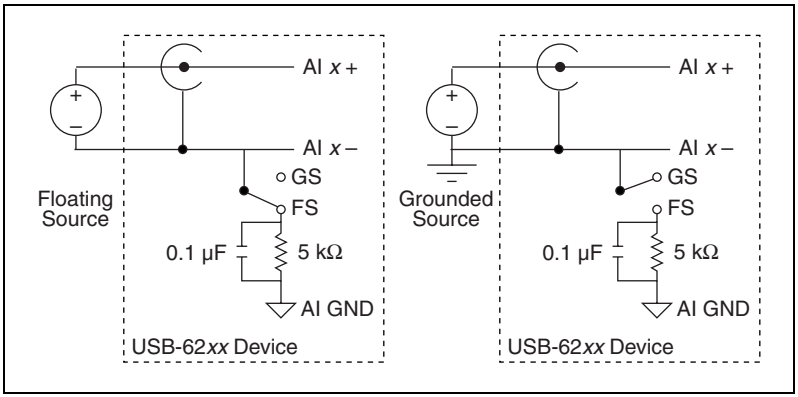

Figure A-48. Analog Input Circuitry

Single-Ended Signals

For each BNC connector that you use for two single-ended channels, set the source type switch to the GS position. This setting disconnects the built-in ground reference resistor from the negative terminal of the BNC connector, allowing the connector to be used as a single-ended channel, as shown in Figure A-49.

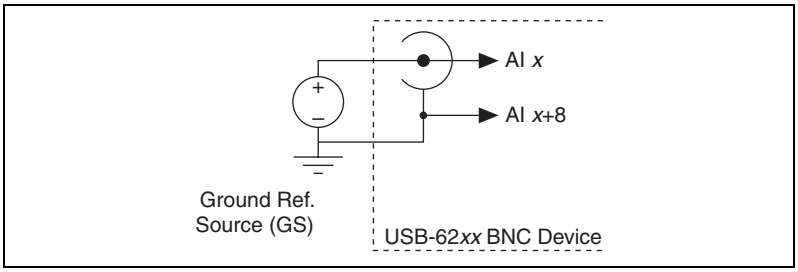

Figure A-49. Single-Ended Channels

When you set the source type to the GS position and configure the device for single-ended input in software, each BNC connector provides access to two single-ended channels, AI *x* and AI *x*+8. For example, the BNC connector labeled AI 0 provides access to single-ended channels AI 0 and AI 8, the BNC connector labeled AI 1 provides access to single-ended channels AI 1 and AI 9, and so on. Up to 32 single-ended channels are available in single-ended measurement modes.

For information on how to connect your single-ended signals, AI GND, and/or AI SENSE, refer to the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*. For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Analog Output

You can access analog output signals on the BNC connectors labeled AO 0 and AO 1. Figure A-50 shows the analog output circuitry on the USB-6259 BNC.

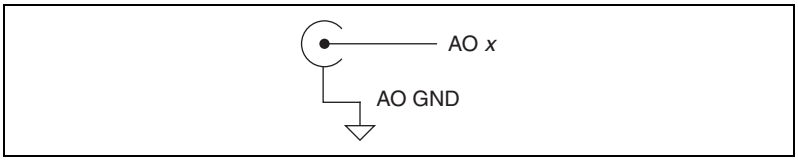

Figure A-50. Analog Output Circuitry

Refer to the *Connecting Analog Output Signals* section of Chapter 5, *Analog Output*, for more information.

Digital I/O and Timing I/O

You can access digital I/O and timing I/O signals on the BNC connectors labeled PFI <0..7>/P1.<0..7>. Figure A-51 shows the DIO/TIO circuitry on the USB-6259 BNC.

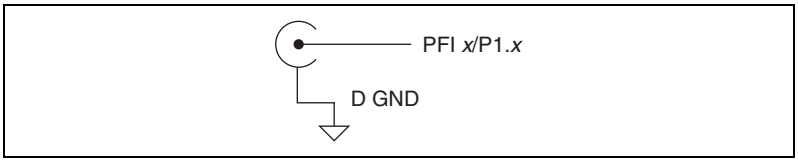

Figure A-51. Digital I/O and Timing I/O Circuitry

Refer to the *Connecting Digital I/O Signals* section of Chapter 6, *Digital I/O*, and the *Connecting PFI Input Signals* section of Chapter 8, *PFI*, for more information.

APFI

You can access the analog programmable function interface signals on the BNC connectors labeled APFI <0..1>. Figure A-52 shows the APFI circuitry on the USB-6259 BNC.

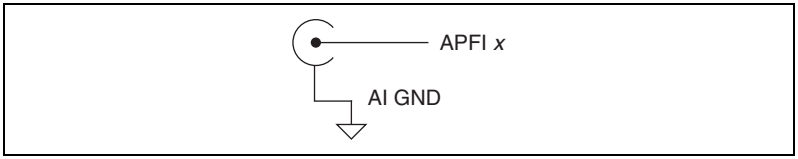

Figure A-52. Analog Programmable Function Interface Circuitry

Refer to the *Triggering with an Analog Source* section of Chapter 11, *Triggering*, for more information.

USER 1 and USER 2

The USER 1 and USER 2 BNC connectors allow you to use a BNC connector for a digital or timing I/O signal of your choice. The USER 1 and USER 2 BNC connectors are routed (internal to the USB-6259 BNC) to the USER 1 and USER 2 screw terminals, as shown in Figure A-53.

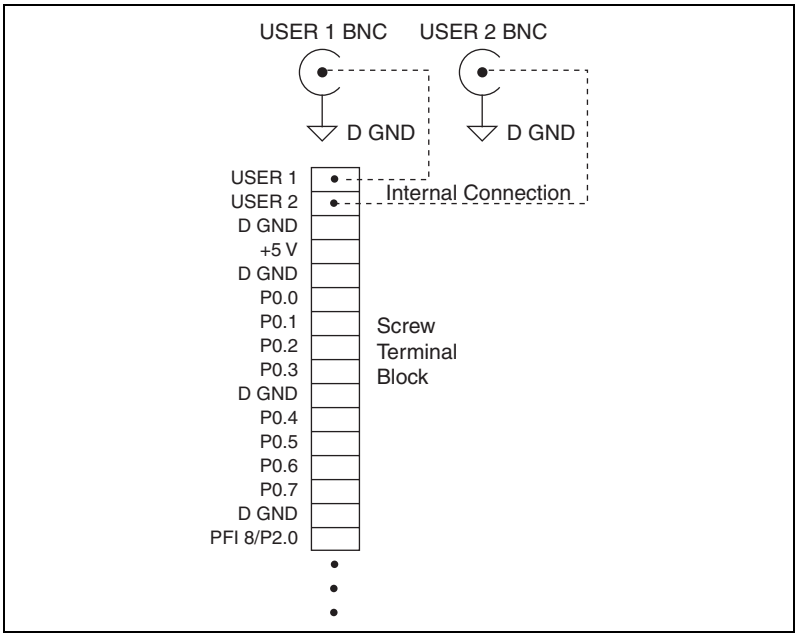

Figure A-53. USER 1 and USER 2 BNC Connections

Figure A-54 shows an example of how to use the USER 1 and USER 2 BNCs. To access the PFI 8 signal from a BNC, connect USER 1 on the screw terminal block to PFI 8 with a wire.

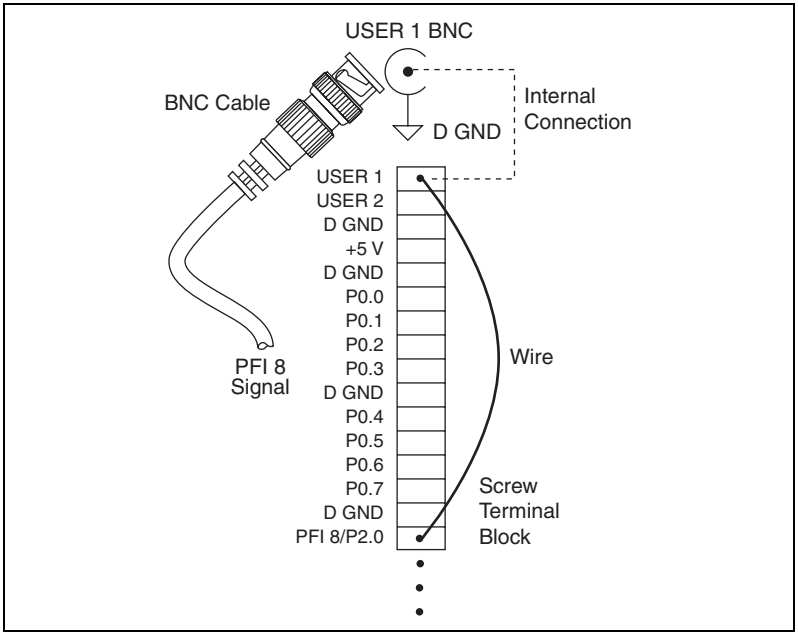

Figure A-54. Connecting PFI 8 to USER 1 BNC

The designated space below each USER <1..2> BNC is for marking or labeling signal names.

USB-6259 BNC Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6259 BNC device.

USB-6259 BNC LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6259 BNC LEDs.

USB-6259 BNC Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6259 BNC.

USB-6259 Mass Termination

USB-6259 Mass Termination Pinout

Figure A-55 shows the pinout of the USB-6259 Mass Termination device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

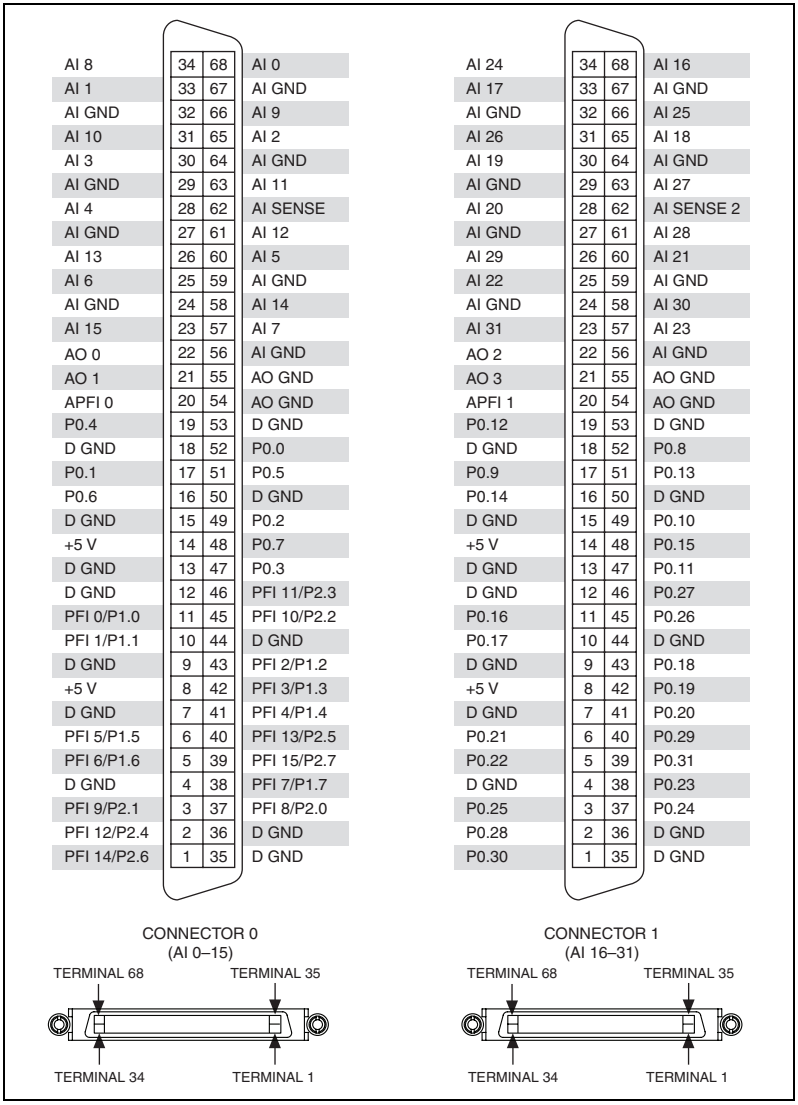

Figure A-55. USB-6259 Mass Termination Pinout

Table A-25. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6259 Mass Termination Specifications

Refer to the *NI 625x Specifications* for more detailed information about the USB-6259 Mass Termination device.

USB-6259 Mass Termination Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the USB-6259 Mass Termination device. Refer to `ni.com` for other accessory options, including new devices.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SH68-68-EP shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SH68-68-EP shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH68-68-EP shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

Cables

In most applications, you can use the following cables:

- **SH68-68-EP**—High-performance cable with individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **R68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6259 Mass Termination LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6259 Mass Termination LEDs.

USB-6259 Mass Termination Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6259 Mass Termination.

NI 6280

PCI/PXI-6280 Pinout

Figure A-56 shows the pinout of the PCI/PXI-6280.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

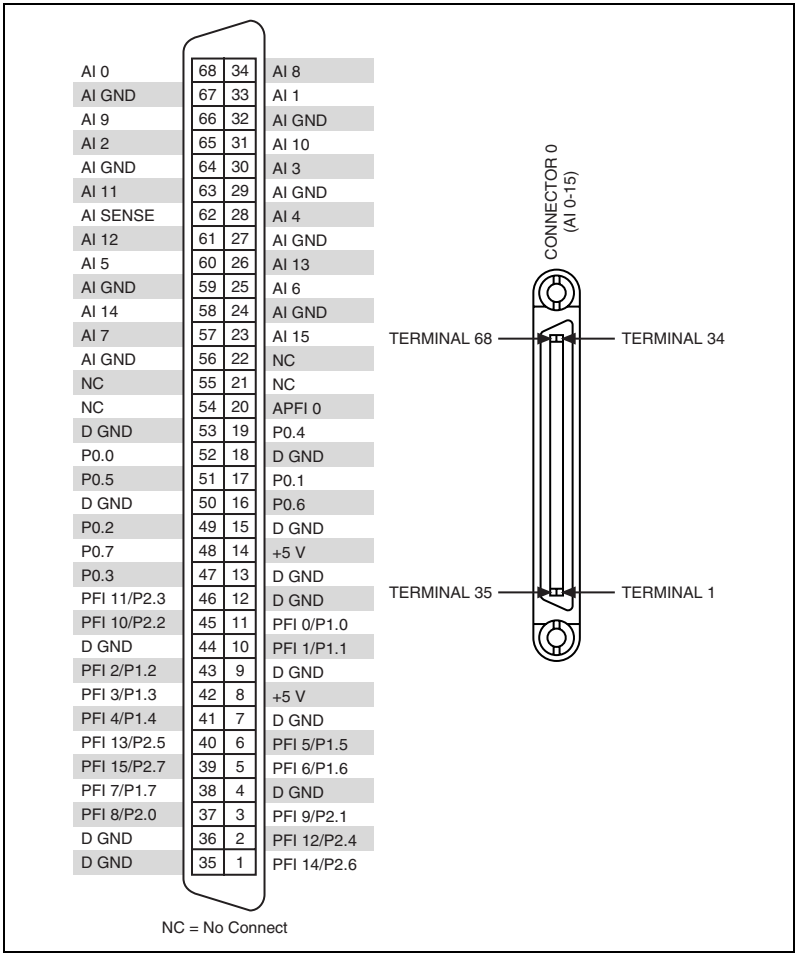

Figure A-56. PCI/PXI-6280 Pinout

Table A-26. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6280 Specifications

Refer to the *NI 628x Specifications* for more detailed information about the PCI/PXI-6280 device.

PCI/PXI-6280 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the PCI/PXI-6280. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706 front panel mounted terminal block for PXI M Series devices

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

NI 6281

The following sections contain information about the PCI/PXI-6281, USB-6281 Screw Terminal, and USB-6281 Mass Termination devices.

PCI/PXI-6281

PCI/PXI-6281 Pinout

Figure A-57 shows the pinout of the PCI/PXI-6281.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

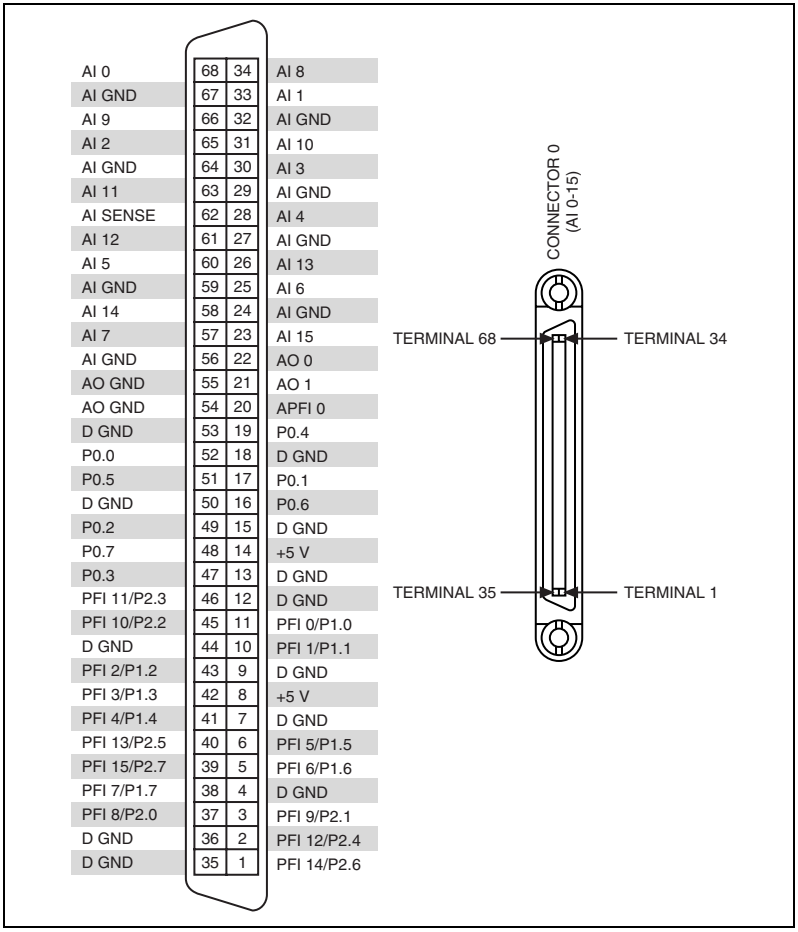

Figure A-57. PCI/PXI-6281 Pinout

Table A-27. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6281 Specifications

Refer to the *NI 628x Specifications* for more detailed information about the PCI/PXI-6281 device.

PCI/PXI-6281 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the PCI/PXI-6281. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

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Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
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Custom Cabling and Connectivity

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Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6281 Screw Terminal

USB-6281 Screw Terminal Pinout

Figure A-29 shows the pinout of the USB-6281 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

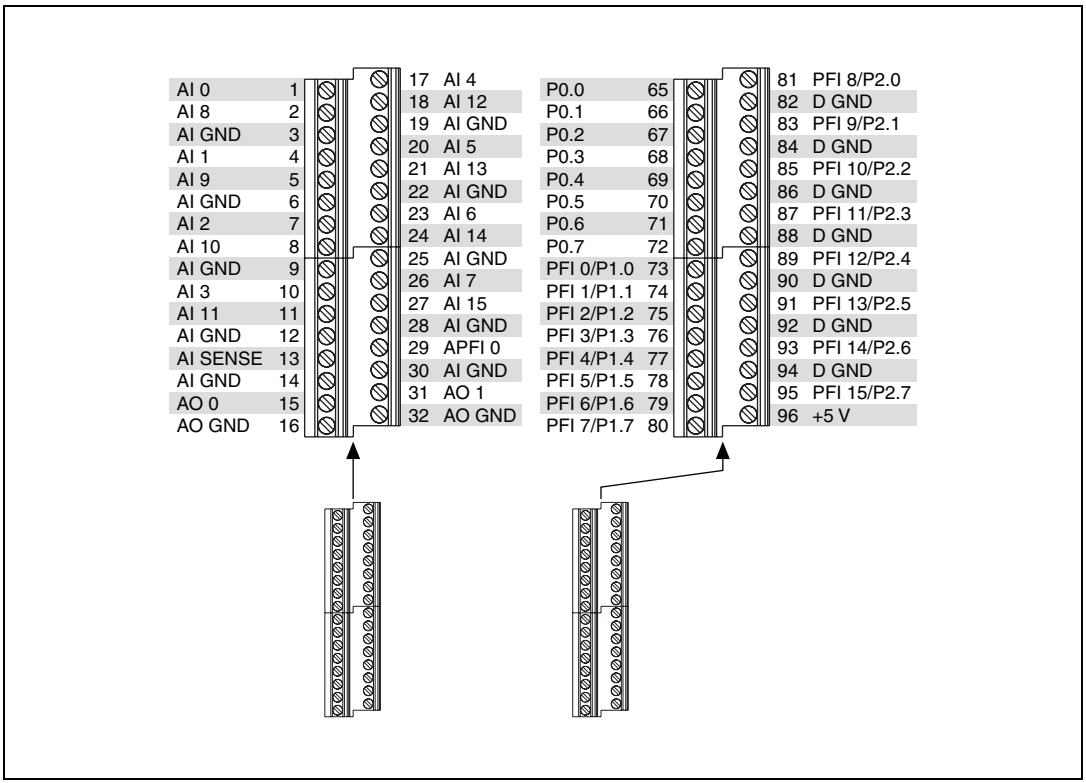


Figure A-58. USB-6281 Screw Terminal Pinout

Table A-28. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	81 (PFI 8)
CTR 0 GATE	83 (PFI 9)
CTR 0 AUX	85 (PFI 10)
CTR 0 OUT	89 (PFI 12)
CTR 0 A	81 (PFI 8)
CTR 0 Z	83 (PFI 9)
CTR 0 B	85 (PFI 10)
CTR 1 SRC	76 (PFI 3)
CTR 1 GATE	77 (PFI 4)
CTR 1 AUX	87 (PFI 11)
CTR 1 OUT	91 (PFI 13)
CTR 1 A	76 (PFI 3)
CTR 1 Z	77 (PFI 4)
CTR 1 B	87 (PFI 11)
FREQ OUT	93 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6281 Screw Terminal Specifications

Refer to the *NI 628x Specifications* for more detailed information about the USB-6281 Screw Terminal device.

USB-6281 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6281 Screw Terminal LEDs.

USB-6281 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6281 Screw Terminal.

USB-6281 Mass Termination

USB-6281 Mass Termination Pinout

Figure A-39 shows the pinout of the USB-6281 Mass Termination device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

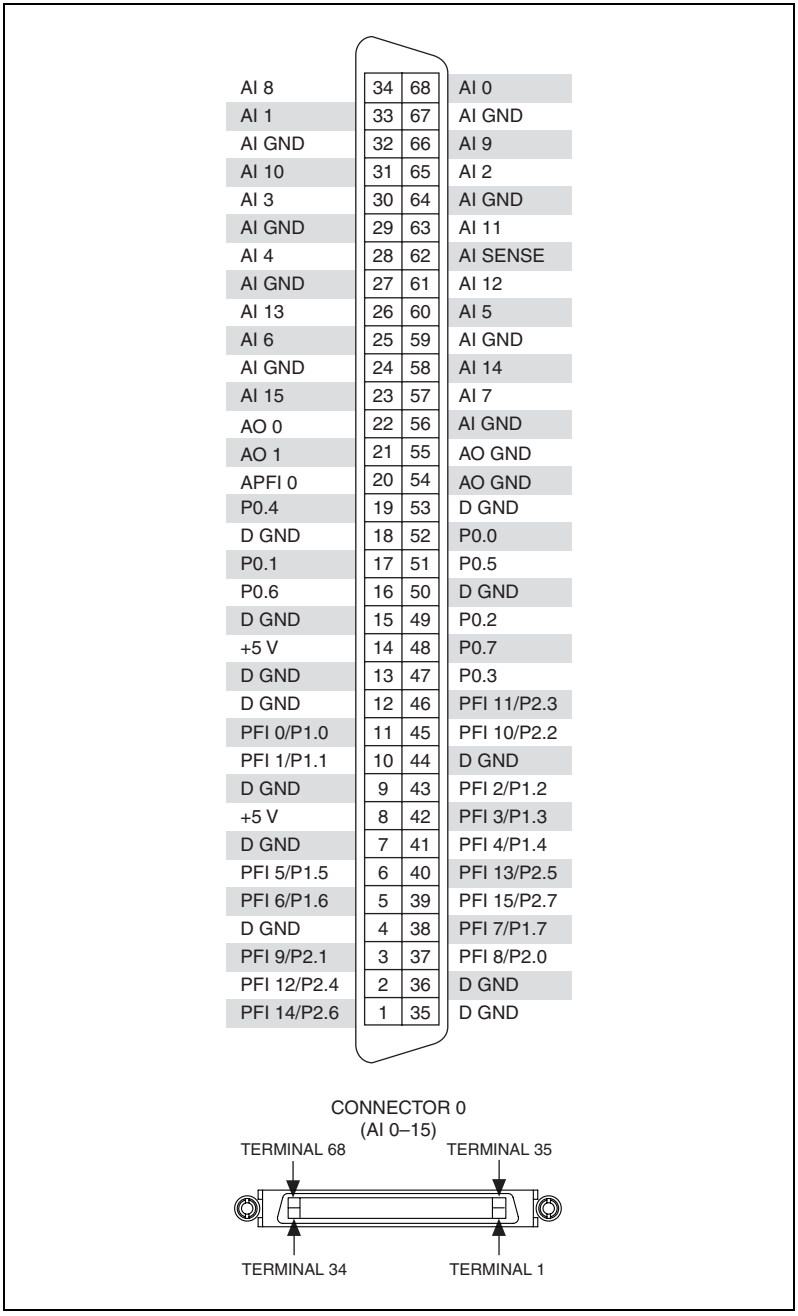


Figure A-59. USB-6281 Mass Termination Pinout

Table A-29. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6281 Mass Termination Specifications

Refer to the *NI 628x Specifications* for more detailed information about the USB-6281 Mass Termination device.

USB-6281 Mass Termination Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with one 68-pin connector, such as the USB-6281 Mass Termination device. Refer to `ni.com` for other accessory options, including new devices.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SH68-68-EP shielded cable.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SH68-68-EP shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output
- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH68-68-EP shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block

Cables

In most applications, you can use the following cables:

- **SH68-68-EP**—High-performance cable with individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **R68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6281 Mass Termination LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6281 Mass Termination LEDs.

USB-6281 Mass Termination Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6281 Mass Termination.

NI 6284

PCI/PXI-6284 Pinout

Figure A-60 shows the pinout of the PCI/PXI-6284. The I/O signals appear on two 68-pin connectors.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

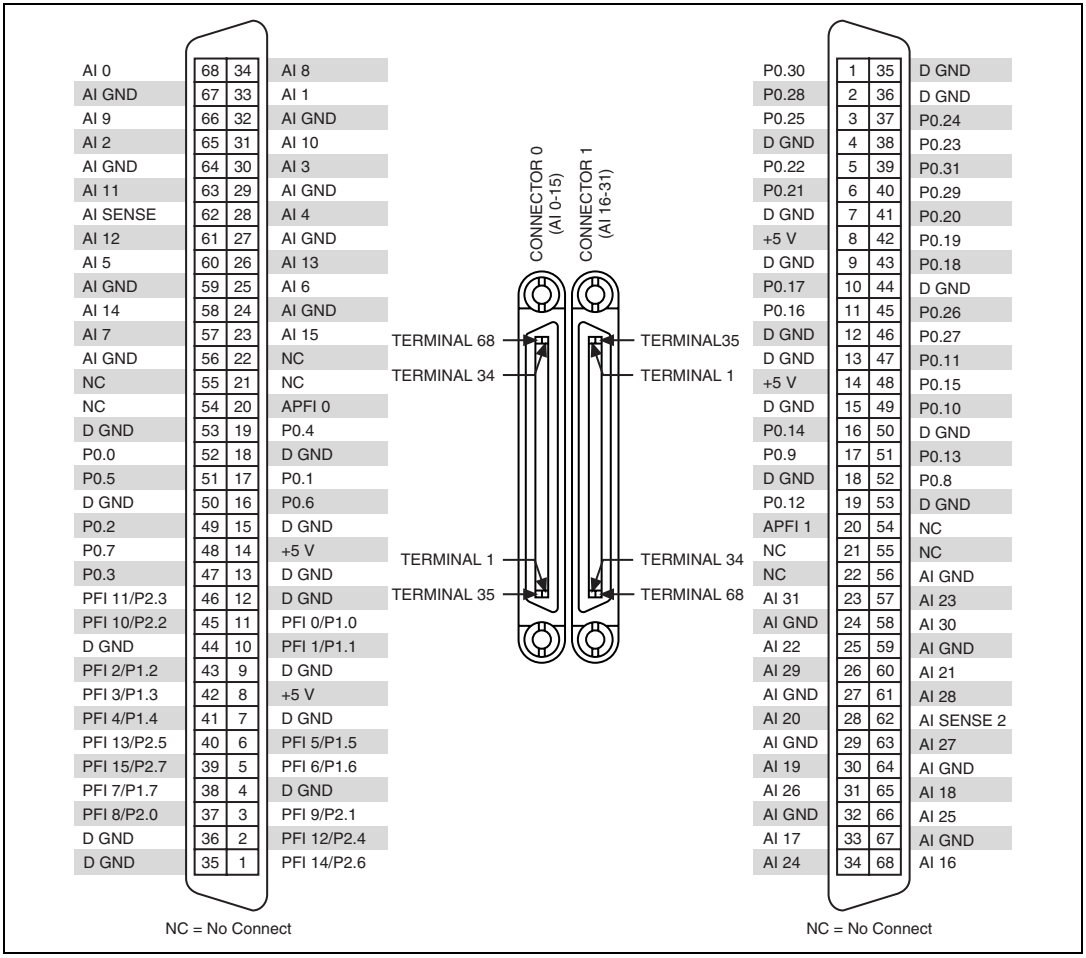


Figure A-60. PCI/PXI-6284 Pinout

Table A-30. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6284 Specifications

Refer to the *NI 628x Specifications* for more detailed information about the PCI/PXI-6284 device.

PCI/PXI-6284 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the PCI/PXI-6284. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. NI-DAQ 7.4 and later supports SCXI in parallel mode on Connector 1.

Note When using Connector 1 in parallel mode with SCXI modules that support track and hold, you must programmatically disable track and hold.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output

- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706[1] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

[1] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

NI 6289

The following sections contain information about the PCI/PXI-6289, USB-6289 Screw Terminal, and USB-6289 Mass Termination devices.

PCI/PXI-6289

PCI/PXI-6289 Pinout

Figure A-61 shows the pinout of the PCI/PXI-6289. The I/O signals appear on two 68-pin connectors.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

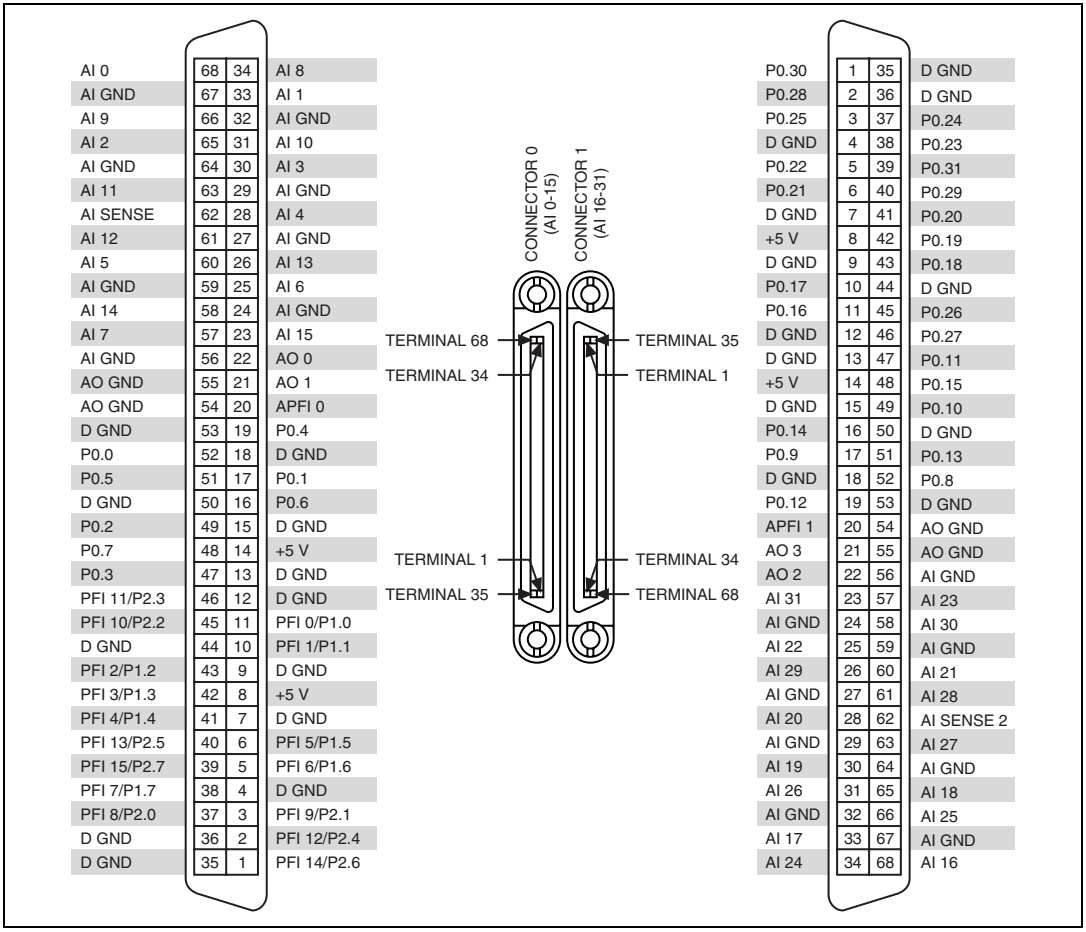


Figure A-61. PCI/PXI-6289 Pinout

Table A-31. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

PCI/PXI-6289 Specifications

Refer to the *NI 628x Specifications* for more detailed information about the PCI/PXI-6289 device.

PCI/PXI-6289 Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the PCI/PXI-6289. Refer to `ni.com` for other accessory options, including new devices.

SCXI Accessories

SCXI is a programmable signal conditioning system designed for measurement and automation applications. To connect your M Series device to an SCXI chassis, use the SCXI-1349 adapter and an SHC68-68-EPM cable.

Use Connector 0 of your M Series device to control SCXI. NI-DAQ 7.4 and later supports SCXI in parallel mode on Connector 1.

Note When using Connector 1 in parallel mode with SCXI modules that support track and hold, you must programmatically disable track and hold.

You also can use an M Series device to control the SCXI section of a PXI/SCXI combination chassis, such as the PXI-1010 or PXI-1011. The M Series device in the rightmost PXI slot controls the SCXI devices. No cables or adapters are necessary.

Refer to the *SCXI Advisor*, available by going to `ni.com/info` and entering the info code `rdscad`, for more information.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SHC68-68-EPM shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SHC68-68-EPM shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
- **BNC-2111**—Provides BNC connectivity to 16 single-ended analog input signals, two analog output signals, five DIO/PFI signals, and the external reference voltage for analog output

- **BNC-2120**—Similar to the BNC-2110, and also has a built-in function generator, quadrature encoder, temperature reference, and thermocouple connector
- **BNC-2090A**—Desktop/rack-mountable device with 22 BNCs for connecting analog, digital, and timing signals

You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SHC68-68-EPM shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block
- TB-2706[1] front panel mounted terminal block for PXI M Series devices

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

RTSI Cables

Use RTSI bus cables to connect timing and synchronization signals among PCI devices, such as M Series, E Series, CAN, and other measurement, vision, and motion devices. Since PXI devices use PXI backplane signals for timing and synchronization, no cables are required.

[1] TB-2706 uses Connector 0 of your PXI device. After a TB-2706 is installed, Connector 1 cannot be used.

Cables

In most applications, you can use the following cables:

- **SHC68-68-EPM**[1]—High-performance cable designed specifically for M Series devices. It has individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **SHC68-68**—Lower-cost shielded cable with 34 twisted pairs of wire
- **RC68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

[1] NI recommends that you use the SHC68-68-EPM cable; however, an SHC68-68-EP cable will work with M Series devices.

USB-6289 Screw Terminal

USB-6289 Screw Terminal Pinout

Figure A-45 shows the pinout of the USB-6289 Screw Terminal.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

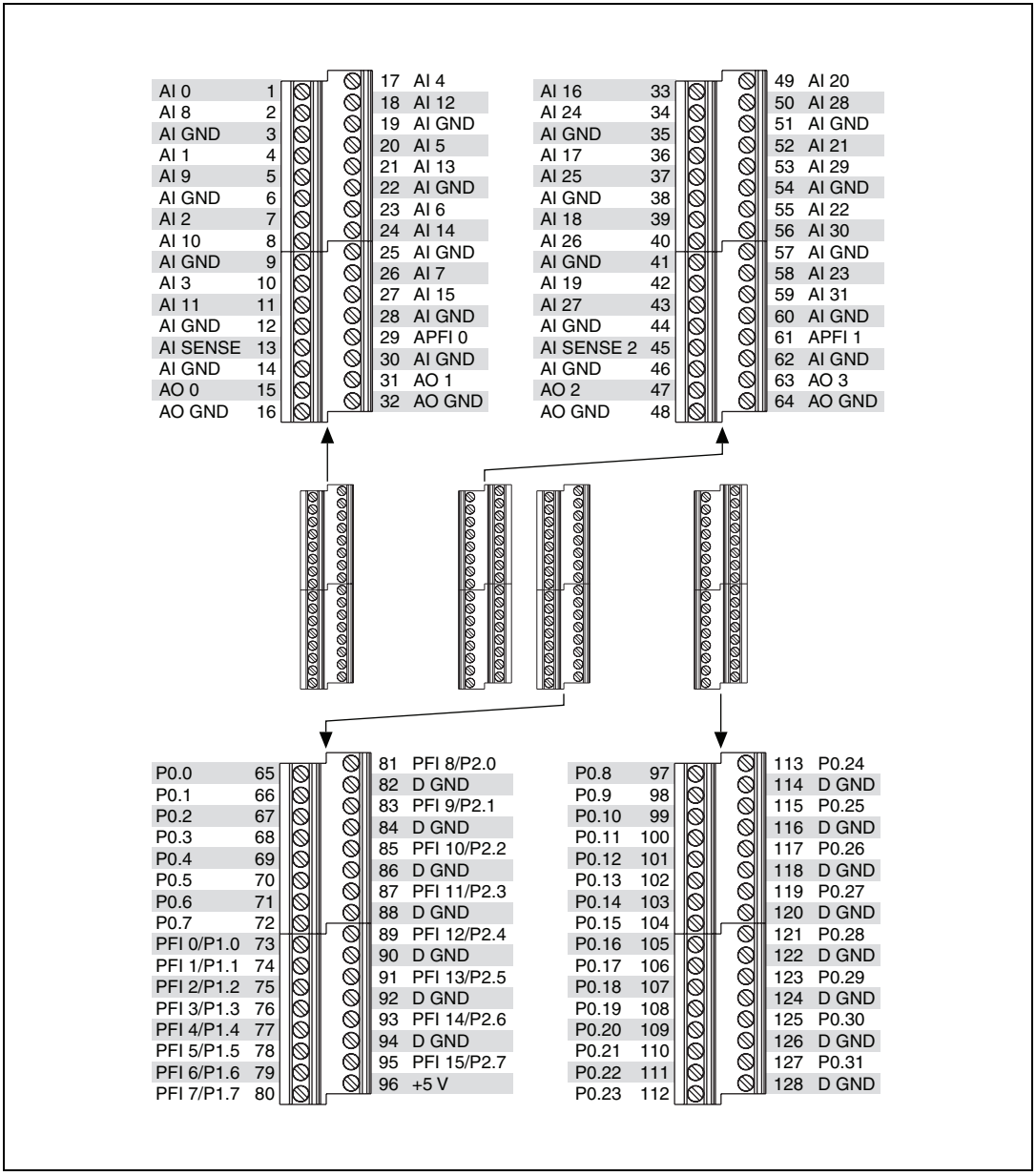


Figure A-62. USB-6289 Screw Terminal Pinout

Table A-32. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Pin Number (Name)
CTR 0 SRC	81 (PFI 8)
CTR 0 GATE	83 (PFI 9)
CTR 0 AUX	85 (PFI 10)
CTR 0 OUT	89 (PFI 12)
CTR 0 A	81 (PFI 8)
CTR 0 Z	83 (PFI 9)
CTR 0 B	85 (PFI 10)
CTR 1 SRC	76 (PFI 3)
CTR 1 GATE	77 (PFI 4)
CTR 1 AUX	87 (PFI 11)
CTR 1 OUT	91 (PFI 13)
CTR 1 A	76 (PFI 3)
CTR 1 Z	77 (PFI 4)
CTR 1 B	87 (PFI 11)
FREQ OUT	93 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6289 Screw Terminal Specifications

Refer to the *NI 628x Specifications* for more detailed information about the USB-6289 Screw Terminal device.

USB-6289 Screw Terminal LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6289 Screw Terminal LEDs.

USB-6289 Screw Terminal Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6289 Screw Terminal.

USB-6289 Mass Termination

USB-6289 Mass Termination Pinout

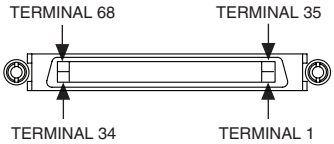
Figure A-55 shows the pinout of the USB-6289 Mass Termination device.

For a detailed description of each signal, refer to the *I/O Connector Signal Descriptions* section of Chapter 3, *Connector and LED Information*.

Note M Series devices may be used with most E Series accessories. However, some E Series accessories use different terminal names. Refer to the *M Series and E Series Pinout Comparison* section of Chapter 3, *Connector and LED Information*, for more information.

AI 8	34	68	AI 0
AI 1	33	67	AI GND
AI GND	32	66	AI 9
AI 10	31	65	AI 2
AI 3	30	64	AI GND
AI GND	29	63	AI 11
AI 4	28	62	AI SENSE
AI GND	27	61	AI 12
AI 13	26	60	AI 5
AI 6	25	59	AI GND
AI GND	24	58	AI 14
AI 15	23	57	AI 7
AO 0	22	56	AI GND
AO 1	21	55	AO GND
APFI 0	20	54	AO GND
P0.4	19	53	D GND
D GND	18	52	P0.0
P0.1	17	51	P0.5
P0.6	16	50	D GND
D GND	15	49	P0.2
+5 V	14	48	P0.7
D GND	13	47	P0.3
D GND	12	46	PFI 11/P2.3
PFI 0/P1.0	11	45	PFI 10/P2.2
PFI 1/P1.1	10	44	D GND
D GND	9	43	PFI 2/P1.2
+5 V	8	42	PFI 3/P1.3
D GND	7	41	PFI 4/P1.4
PFI 5/P1.5	6	40	PFI 13/P2.5
PFI 6/P1.6	5	39	PFI 15/P2.7
D GND	4	38	PFI 7/P1.7
PFI 9/P2.1	3	37	PFI 8/P2.0
PFI 12/P2.4	2	36	D GND
PFI 14/P2.6	1	35	D GND

CONNECTOR 0
(AI 0–15)



AI 24	34	68	AI 16
AI 17	33	67	AI GND
AI GND	32	66	AI 25
AI 26	31	65	AI 18
AI 19	30	64	AI GND
AI GND	29	63	AI 27
AI 20	28	62	AI SENSE 2
AI GND	27	61	AI 28
AI 29	26	60	AI 21
AI 22	25	59	AI GND
AI GND	24	58	AI 30
AI 31	23	57	AI 23
AO 2	22	56	AI GND
AO 3	21	55	AO GND
APFI 1	20	54	AO GND
P0.12	19	53	D GND
D GND	18	52	P0.8
P0.9	17	51	P0.13
P0.14	16	50	D GND
D GND	15	49	P0.10
+5 V	14	48	P0.15
D GND	13	47	P0.11
D GND	12	46	P0.27
P0.16	11	45	P0.26
P0.17	10	44	D GND
D GND	9	43	P0.18
+5 V	8	42	P0.19
D GND	7	41	P0.20
P0.21	6	40	P0.29
P0.22	5	39	P0.31
D GND	4	38	P0.23
P0.25	3	37	P0.24
P0.28	2	36	D GND
P0.30	1	35	D GND

CONNECTOR 1
(AI 16–31)

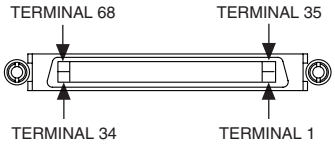


Figure A-63. USB-6289 Mass Termination Pinout

Table A-33. Default NI-DAQmx Counter/Timer Pins

Counter/Timer Signal	Default Connector 0 Pin Number (Name)
CTR 0 SRC	37 (PFI 8)
CTR 0 GATE	3 (PFI 9)
CTR 0 AUX	45 (PFI 10)
CTR 0 OUT	2 (PFI 12)
CTR 0 A	37 (PFI 8)
CTR 0 Z	3 (PFI 9)
CTR 0 B	45 (PFI 10)
CTR 1 SRC	42 (PFI 3)
CTR 1 GATE	41 (PFI 4)
CTR 1 AUX	46 (PFI 11)
CTR 1 OUT	40 (PFI 13)
CTR 1 A	42 (PFI 3)
CTR 1 Z	41 (PFI 4)
CTR 1 B	46 (PFI 11)
FREQ OUT	1 (PFI 14)

Note For more information about default NI-DAQmx counter inputs, refer to *Connecting Counter Signals* in the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

USB-6289 Mass Termination Specifications

Refer to the *NI 628x Specifications* for more detailed information about the USB-6289 Mass Termination device.

USB-6289 Mass Termination Accessory and Cabling Options

This section describes some cable and accessory options for M Series devices with two 68-pin connectors, such as the USB-6289 Mass Termination device. Refer to `ni.com` for other accessory options, including new devices.

SCC Accessories

SCC provides portable, modular signal conditioning to your DAQ system. To connect your M Series device to an SCC module carrier, such as the SC-2345, SC-2350, or SCC-68, use an SH68-68-EP shielded cable.

Use Connector 0 of your M Series device to control an SCC module carrier. SCC carriers can be used with Connector 1 with NI-DAQ 7.4 and later.

Refer to the *SCC Advisor*, available by going to `ni.com/info` and entering the info code `rdscav`, for more information.

BNC Accessories

You can use the SH68-68-EP shielded cable, to connect your DAQ device to BNC accessories, such as the following:

- **BNC-2110**—Provides BNC connectivity to all analog signals, some digital signals, and spring terminals for other digital signals
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You can use one BNC accessory with the signals on either connector of your M Series device. You can use two BNC accessories with one M Series device by using both connectors.

Screw Terminal Accessories

National Instruments offers several styles of screw terminal connector blocks. Use an SH68-68-EP shielded cable to connect an M Series device to a connector block, such as the following:

- CB-68LP and CB-68LPR unshielded connector blocks
- SCC-68 I/O connector block with screw terminals, general breadboard area, bus terminals, and four expansion slots for SCC signal conditioning modules
- SCB-68 shielded connector block with temperature sensor
- TBX-68 DIN rail-mountable connector block

You can use one screw terminal accessory with the signals on either connector of your M Series device. You can use two screw terminal accessories with one M Series device by using both connectors.

Cables

In most applications, you can use the following cables:

- **SH68-68-EP**—High-performance cable with individual bundles separating analog and digital signals. Each differential analog input channel is routed on an individually shielded twisted pair of wires. Analog outputs are also individually shielded
- **R68-68**—Highly-flexible unshielded ribbon cable

Custom Cabling and Connectivity

The CA-1000 is a configurable enclosure that gives user-defined connectivity and flexibility through customized panelettes. Visit `ni.com` for more information about the CA-1000.

Refer to the *Custom Cabling* section of Chapter 2, *DAQ System Overview*, for more information about custom cabling solutions.

USB-6289 Mass Termination LED Patterns

Refer to the *LED Patterns* section of Chapter 3, *Connector and LED Information*, for information about the USB-6289 Mass Termination LEDs.

USB-6289 Mass Termination Fuse Replacement

Refer to the *USB Device Fuse Replacement* section of Chapter 3, *Connector and LED Information*, for information about replacing the fuse on the USB-6289 Mass Termination.

B

Timing Diagrams

This appendix contains detailed timing information and diagrams for the M Series device blocks:

- *Analog Input Timing Diagrams*
- *Analog Output Timing Diagrams*
- *Digital I/O Timing Diagrams*
- *Counters Timing Diagrams*
- *Clock Generation Timing Diagrams*

Analog Input Timing Diagrams

The following sections describe the timing specifications and timing of the triggers and clock signals related to the analog input timing engine:

- *Input Timing*—Input timing relates to any signal external to the M Series device that will be used as a clock or a trigger. This timing describes the delays involved with importing the external signal into the device.
- *Internal Timing*—Internal timing describes the relationship between internal signals. In general, how the input and other internal signals get used to generate output signals, such as the convert signal.
- *Output Timing*—Output timing refers to the timing parameters related to exporting signals internal to the device to a terminal for external use.

Figure B-1 is a simplified model of the M Series analog input timing engine.

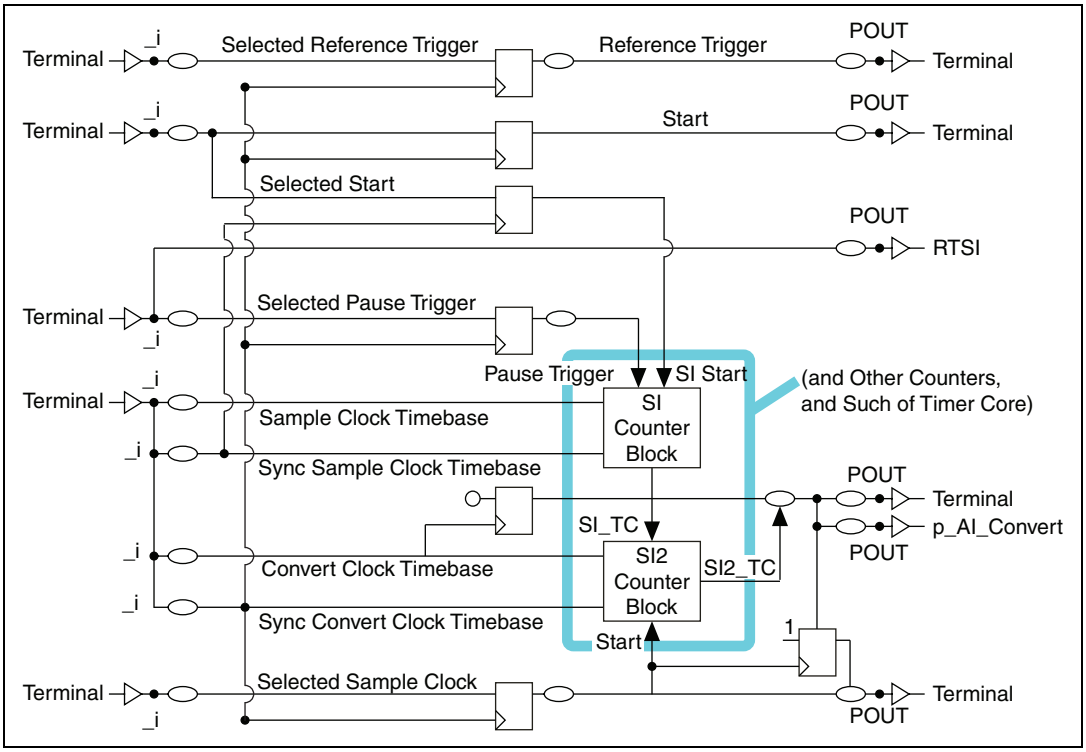

Figure B-1. M Series Analog Input Timing Engine

The following signals are used in Figure B-1 and in the following sections:

- **Terminal**—Refers to any device terminal, such as PFI or RTSI. These terminals are used as inputs and as outputs for signals.
- **_i**—Refers to any internal signal available to the analog input timing engine for use. In the case of signals coming from an external terminal, this would be the signal after is been through the first input buffer. _i also can refer to other internal signals such as internal timebases or signals coming from other blocks.
- **POUT**—Refers to any output signal right before it is driven to an output terminal.
- **Convert Clock Timebase and Sync Convert Clock Timebase**—Convert Clock Timebase is the source signal used to generate the signal that will actually cause the ADC to do a conversion (p_AI_Convert). This signal can be an internal or external timebase

that will be divided by the SI2 counter, or can be an external Convert Clock signal. Sync Convert Clock Timebase is a signal related to Convert Clock Timebase that is used to synchronize external signals before they are used by circuits running from Convert Clock Timebase.

- **Sample Clock Timebase and Sync Sample Clock Timebase**—Sample Clock Timebase is the source for the SI counter and can be used to generate the sample timing. Each Sample Clock in turn triggers the generation of one or more converts. This signal can be an internal or external timebase. Sync Sample Clock Timebase is a signal related to Sample Clock Timebase that is used to synchronize external signals before they are used by circuits running from Sample Clock Timebase.
- **Selected Start and Start**—Start is the signal that starts the analog input timing engine. This signal can come from external signals, a software command, or internal sources. Selected Start is the signal chosen to be the Start before it is synchronized (just after the selection mux).
- **Selected Reference Trigger and Reference Trigger**—A Reference Trigger is a trigger that can stop the AI timing engine. If the Reference Trigger is enabled, the AI timing engine will stop acquiring data once it sees a valid event on the Reference Trigger and it has acquired the posttrigger number of samples. This signal can come from external signals, a software command, or internal sources. The Selected Reference Trigger is the signal chosen to be the Reference Trigger before it is synchronized (just after the selection mux).
- **Selected Sample Clock and Sample Clock**—Selected Sample Clock is the signal selected to become Sample Clock before any synchronization (just after the selection mux). The Sample Clock marks the beginning of a new sample. This signal can be an external or internal signal. When an internal signal, it can be generated with the SI counter dividing the Sample Clock Timebase signal. It also can come from an external terminal or from a signal from another internal resource inside the M Series device.
- **Selected Pause Trigger and Pause Trigger**—The Pause Trigger can be used to pause the acquisition for a certain period of time. Selected Pause Trigger is the signal that becomes the Pause Trigger signal before synchronization.
- **p_AI_Convert**—The signal that starts the conversions of data at the ADC component. This signal goes directly to the ADC, but copies can be routed to output terminals.

Input Timing

Input timing refers to the delays involved in importing external signals to be used as triggers or clocks in the AI timing engine. Figures B-2 and B-3 and Table B-1 describe the insertion delays for external signals.

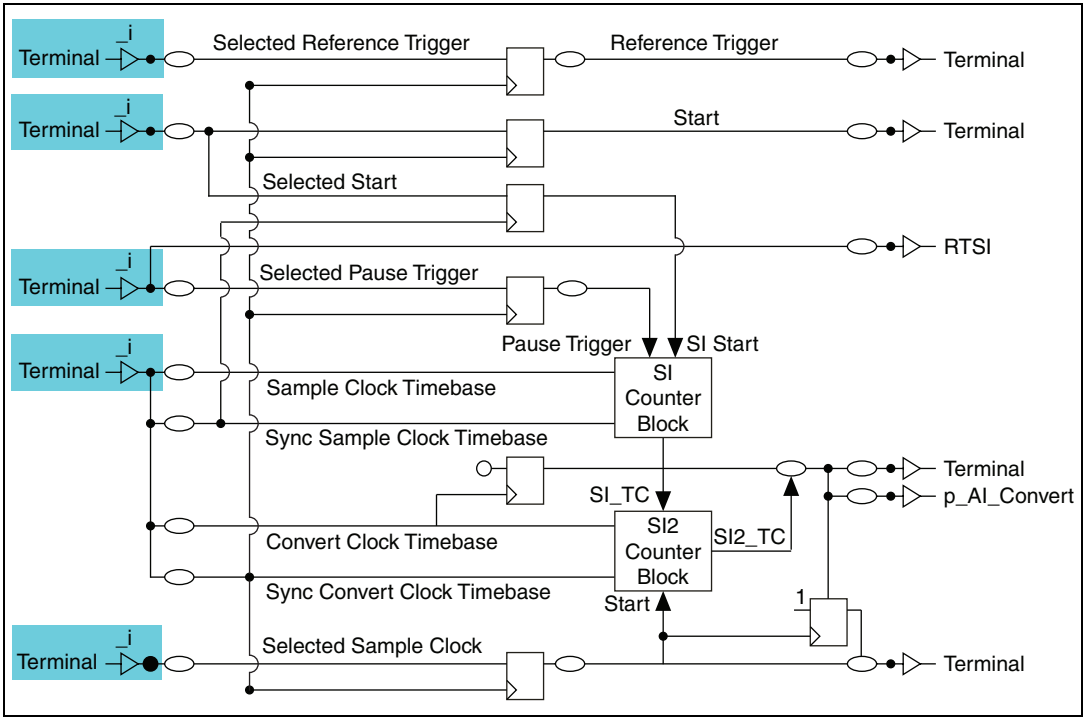

Figure B-2. Input Timing and the Analog Input Timing Engine

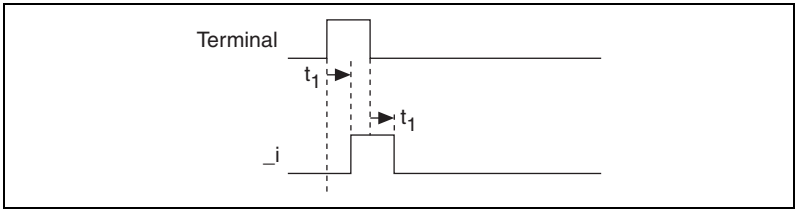

Figure B-3. Input Timing Diagram

Table B-1. Input Timing

Time	From	To	Min (ns)		Max (ns)	
t_1*	PFI	PFI_i	4.2	6.4	15.2	19.2
	RTSI	RTSI_i	0.9	2.2	2.0	3.0
	STAR	STAR_i	0.9	—	—	2.8

* The delay ranges given for PFI and RTSI represent the fastest and slowest terminal routing within the trigger group for a given condition (maximum or minimum timing). This difference can be useful when two external signals will be used together and the relative timing between the signals is important.

Internal Timing

AI Timing Clocks

The analog input timing engine has two levels of timing that control an AI acquisition. The first level is the convert level. This is the timing that controls when the analog to digital conversions take place. The SC, DIV, and SI2 counters run on this timing level. The signal that clocks this timing level is called Convert Clock Timebase. This signal can come from an internal source (for example, an internal timebase) or an external signal. It can be divided down using the SI2 counter, or it can be used directly (in external convert mode). In order to synchronize triggers to the Convert Clock Timebase signal, another related signal is generated called Sync Convert Clock Timebase. Sync Convert Clock Timebase is generated differently depending on the mode the AI timing engine is operating on:

- When Convert Clock Timebase is a signal that will be divided down using the SI2 counter (either internal or external), it is considered to be a free-running clock. In this case, the Sync Convert Clock Timebase is the inverted version of the Convert Clock Timebase signal. The idea is to use the falling edge of the original signal to synchronize external signals before the rising edge of the Convert Clock Timebase occurs (after polarity selection). This case is the one described in this section.
- When Convert Clock Timebase is not going to be divided by the SI2 counter (in the case of an external convert signal), this signal is assumed to be not free-running and highly irregular. In this case, Sync Convert Clock Timebase is selected to be the actual external signal, and Convert Clock Timebase is a delayed version of the external signal. This delay is long enough so that external signals can be synchronized with Sync Convert Clock Timebase and used by Convert Clock Timebase. For timing diagrams and parameters for this case, refer to the *Convert Clock* section.

The second level of timing is the sample level. Basically, converts are grouped in sets called samples, and the timing of the samples can be independent from the timing of the converts. The M Series device can use a timebase to generate the sample timing. This timebase is called Sample Clock Timebase. This signal can be internal (for example, an internal timebase) or external. Either way, the signal gets divided in the SI counter and used to generate Sample Clock signals (which in turn, signal the start of a sample). In order to synchronize external triggers to the Sample Clock Timebase, another related signal is created, Sync Sample Clock Timebase. This is always the inverted signal selected to be Sample Clock Timebase, while the Sample Clock Timebase signal is a copy without inversion of the signal. The idea is that for each significant edge of the Sample Clock Timebase, there is a significant edge of the Sync Sample Clock Timebase signal that occurs before Sample Clock Timebase and that can be used to synchronize the input triggers.

The source for Convert Clock Timebase and Sample Clock Timebase is the internal signal bus, _i. The timing of this signal is described in relation to this common point. The Convert Clock Timebase and Sample Clock Timebase can be asynchronous from each other.

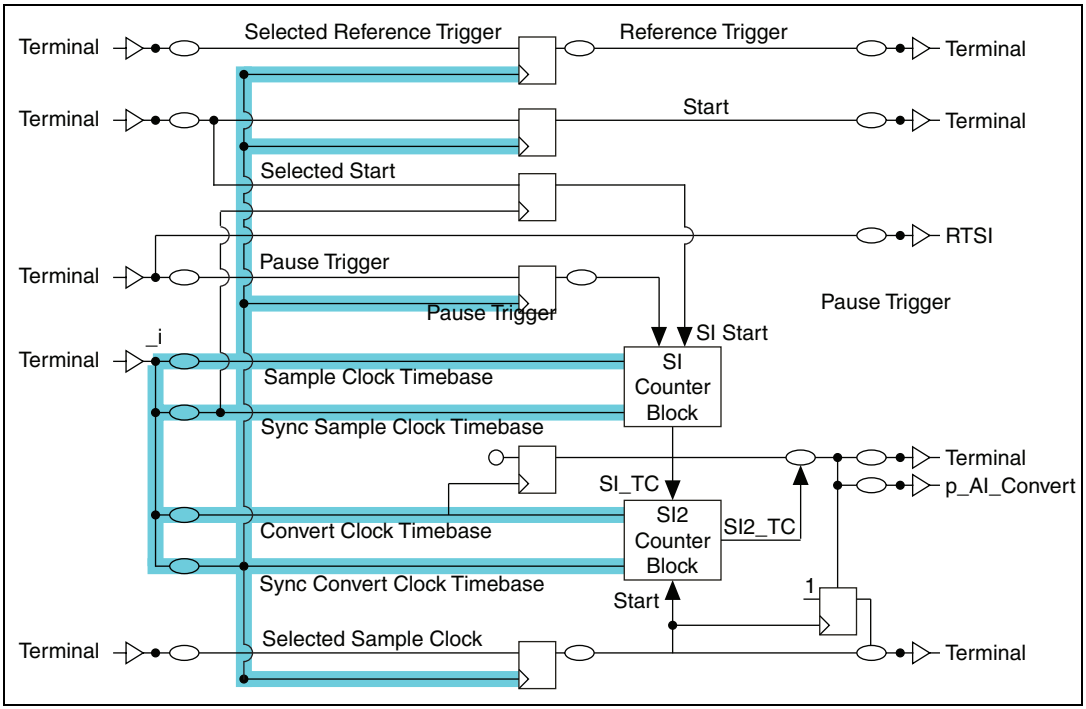

Figure B-4. AI Timing Clocks and the Analog Input Timing Engine

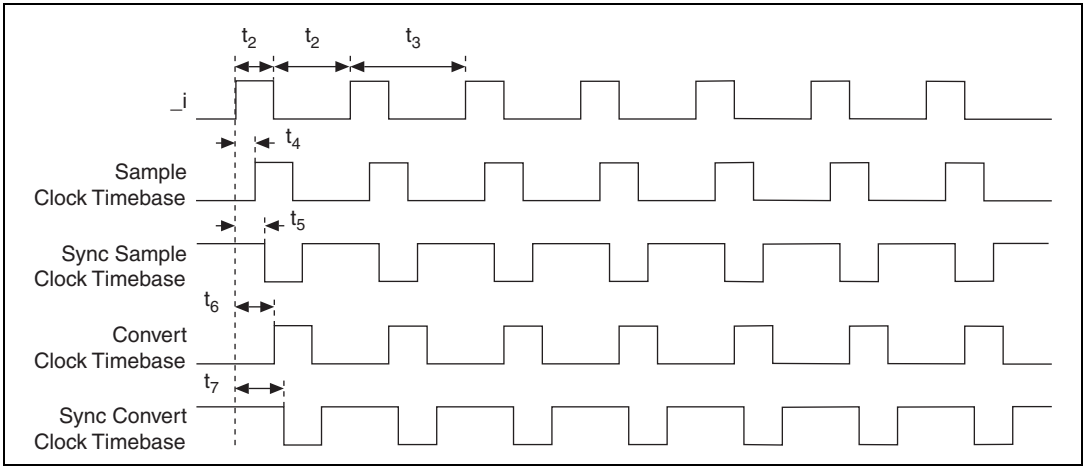

Figure B-5. AI Timing Clocks Timing Diagram

Table B-2. AI Timing Clocks Timing

Time	Description	Line	Min (ns)	Max (ns)
t_2	Minimum Pulse Width	—	12.5	—
t_3	Minimum Period	—	50.0	—
t_4	Delay to Sample Clock Timebase	PFI	3.8	9.3
		RTSI	3.5	9.0
		STAR	3.0	6.4
t_5	Delay to Sync Sample Clock Timebase	PFI	3.4	8.5
		RTSI	3.2	8.3
		STAR	2.7	5.6
t_6	Delay to Convert Clock Timebase	PFI	4.1	10.2
		RTSI	3.9	9.9
		STAR	3.4	7.3
t_7	Delay to Sync Convert Clock Timebase	PFI	3.6	8.9
		RTSI	3.3	8.6
		STAR	2.9	6.0

Convert Clock

Convert Clock is the signal that determines when an analog to digital conversion is started. The signal going to the ADC is called p_AI_Convert. Convert Clock also can be routed to several external I/O terminals for external use. Convert Clock is always generated from the Convert Clock Timebase signal, either directly or indirectly (by dividing it down using the SI2 counter). If the SI2 counter is used, it is assumed that a reliable free-running clock is being used. Refer to the *AI Timing Clocks* section for the timing relationship between Convert Clock Timebase and Sync Convert Clock Timebase. If the SI2 counter is not being used (external convert case), the Convert Clock Timebase is assumed to be not free-running and the relationship between the Convert Clock Timebase and the Sync Convert Clock Timebase is an asynchronous delay.

Whether the SI2 counter is used or not, the timing parameters in the generation of Convert Clock are the same starting at the Convert Clock Timebase signal.

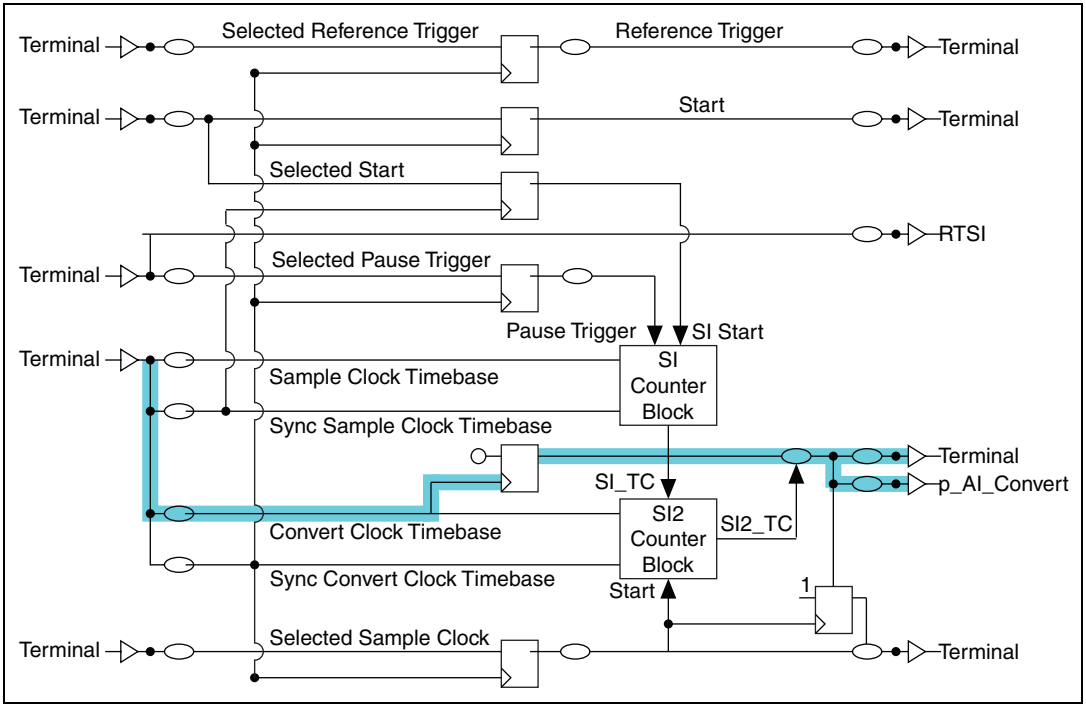

Figure B-6. Convert Clock and the Analog Input Timing Engine

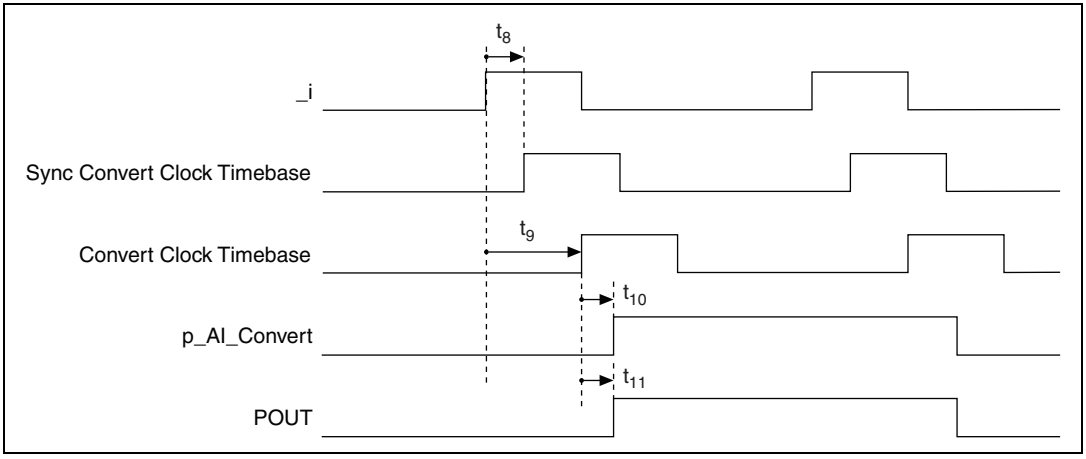

Figure B-7. Convert Clock Timing Diagram

Table B-3. Convert Clock Timing

Time	Description	Line	Min (ns)	Max (ns)
t_8	Delay from _i to Sync Convert Clock Timebase	PFI	6.4	15.9
		RTSI	6.0	15.6
		STAR	5.7	12.9
t_9	Delay from _i to Convert Clock Timebase	PFI	16.2	39.1
		RTSI	16.0	38.8
		STAR	15.5	36.1
t_{10}	Delay from Convert Clock Timebase to p_AI_Convert	—	6.0	13.0
t_{11}	Delay from Convert Clock Timebase to Convert Clock, when exported to an external terminal (POUT)	PFI	4.6	10.8
		RTSI	4.6	10.5

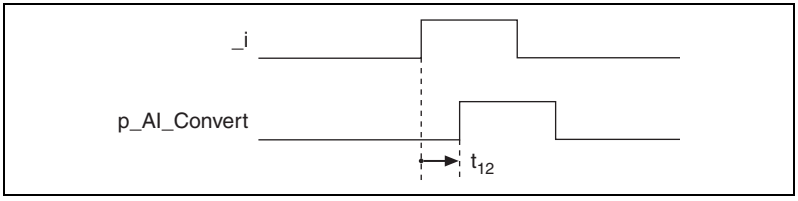

Figure B-8. Convert Clock and Any Internal Signal Timing Diagram

Table B-4. Convert Clock and Any Internal Signal Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{12}	_i to p_AI_Convert in external convert mode	PFI	22.2	52.1
		RTSI	22.1	51.8
		STAR	21.5	49.1

Start

Start is the signal that starts an AI acquisition. This signal can come from an external source (through an external terminal) or from an internal source. One possible internal source is a software-generated pulse. A multiplexer selects from all the possible sources (all of them at _i level) and outputs a signal called Selected Start. Selected Start then gets sent to the two timing levels in the AI section (the Convert Clock Timebase and the Sample Clock Timebase timing level) for synchronization to each clock. Once the Convert Clock Timebase timing domain has received a valid Start, the AI timing engine is ready to start generating converts, as soon as it receives a Sample Clock (beginning of a sample). Once the Sample Clock Timebase domain has received a valid Start, the AI timing engine is ready to start generating Sample Clocks.

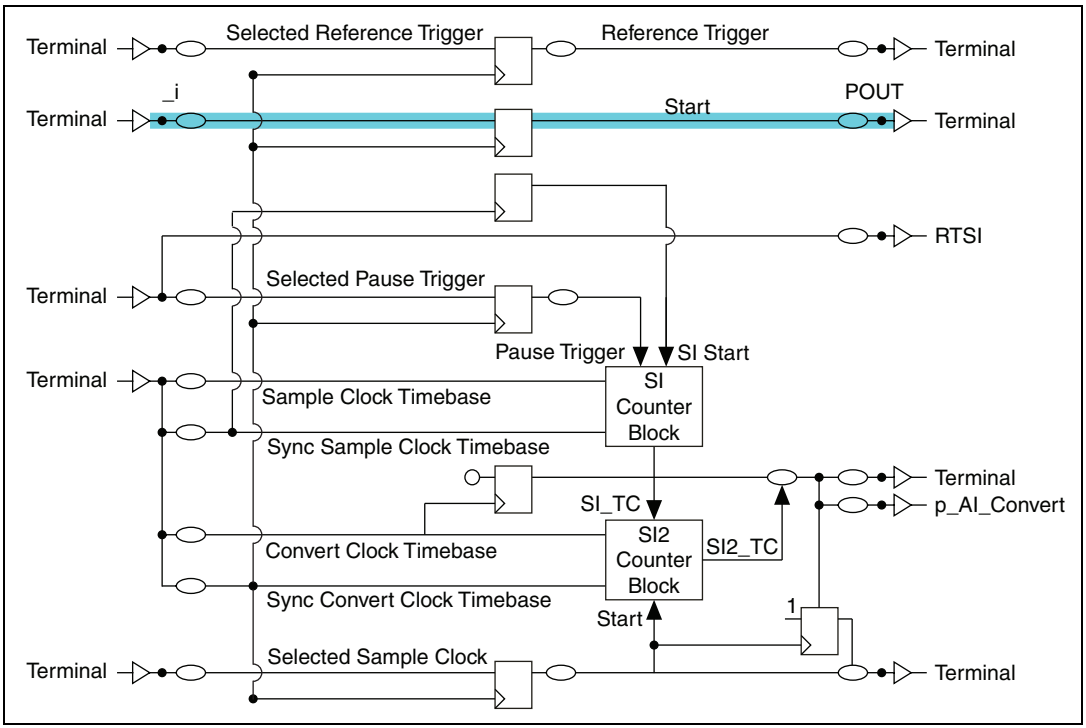

Figure B-9. Convert Clock Timebase Timing and the Analog Input Timing Engine

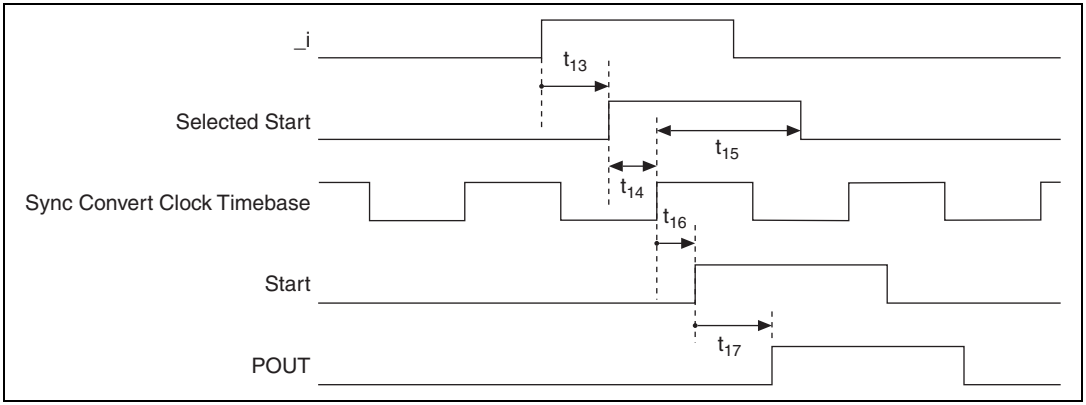

Figure B-10. Convert Clock Timebase Timing Diagram

Table B-5. Convert Clock Timebase Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{13}	Delay to Selected Start	PFI	3.4	8.8
		RTSI	3.3	8.5
		STAR	2.7	5.7
t_{14}	Selected Start Setup Time (to Sync Convert Clock Timebase)	—	1.5	—
t_{15}	Selected Start Hold Time (to Sync Convert Clock Timebase)	—	0	—
t_{16}	Sync Convert Clock Timebase to Start	—	0.9	2.4
t_{17}	Start to POUT	PFI	1.1	3.1
		RTSI	1.1	2.7

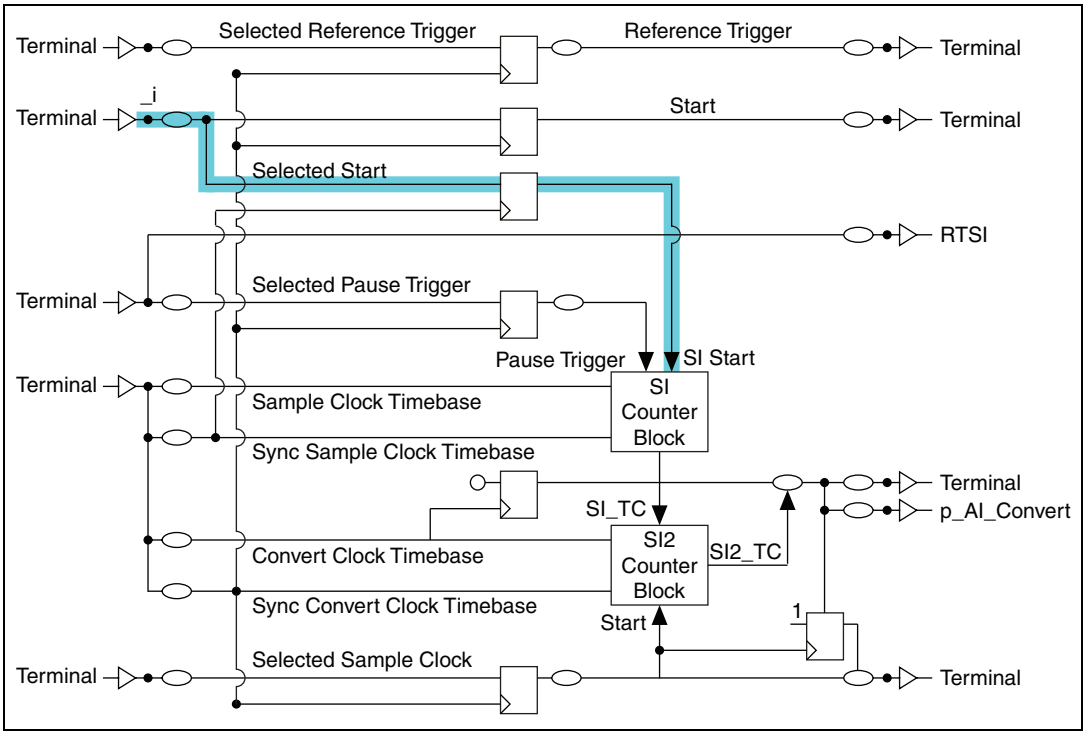

Figure B-11. Sample Clock Timebase Timing and the Analog Input Timing Engine

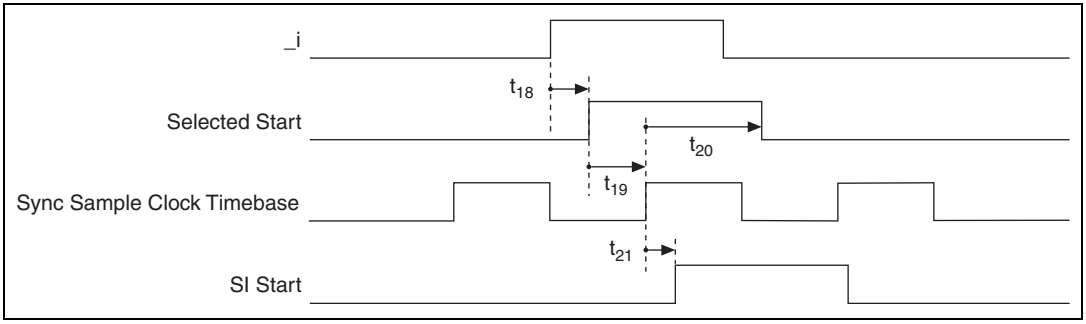

Figure B-12. Sample Clock Timebase Timing Diagram

Table B-6. Sample Clock Timebase Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{18}	Delay to Selected Start	PFI	3.4	8.8
		RTSI	3.3	8.5
		STAR	2.7	5.7
t_{19}	Selected Start Setup/Hold Time (to Sync Sample Clock Timebase)	—	1.5	—
t_{20}	Selected Start Setup/Hold Time (to Sync Sample Clock Timebase)	—	0	—
t_{21}	Sync Sample Clock Timebase to SI_Start	—	0.9	2.2

Reference Trigger

Use the *Reference Trigger* to stop the acquisition. It is normally used in pretrigger acquisitions; it is necessary to acquire data before and after the trigger. The Reference Trigger signals the time when the AI timing engine starts counting the number of posttrigger conversions to take before stopping. The Reference Trigger can come from external or internal sources and its source is selected with a multiplexer. Its output is called the *Selected Reference Trigger.*

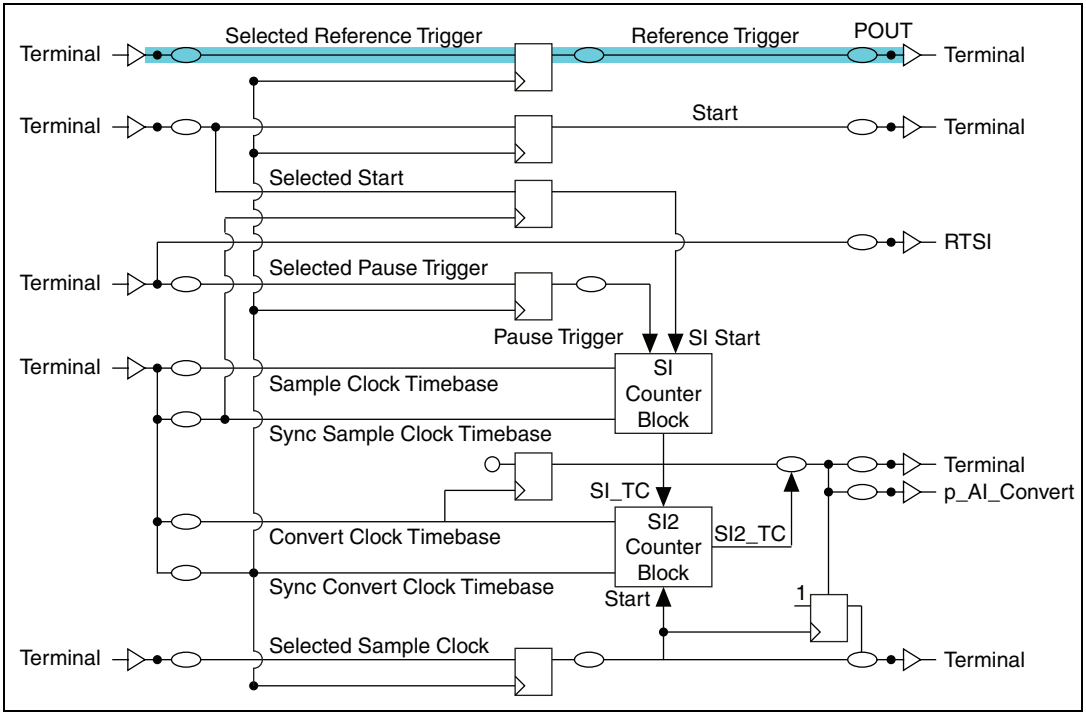

Figure B-13. Reference Trigger and the Analog Input Timing Engine

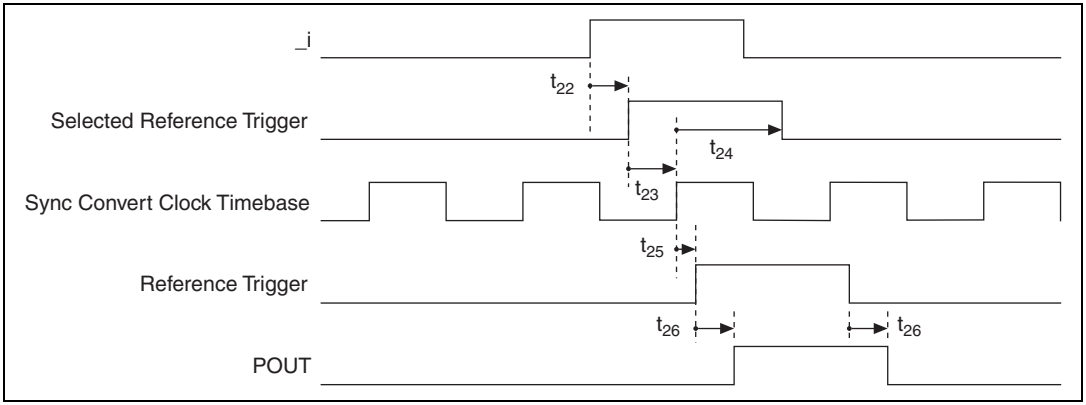

Figure B-14. Reference Trigger Timing Diagram

Table B-7. Reference Trigger Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{22}	Delay to the Selected Reference Trigger	PFI	3.6	8.9
		RTSI	3.4	8.4
		STAR	2.9	5.6
t_{23}	Selected Reference Trigger Setup (to Sync Convert Clock Timebase)	—	1.5	—
t_{24}	Selected Reference Trigger Hold (to Sync Convert Clock Timebase)	—	0	—
t_{25}	Sync Convert Clock Timebase to Reference Trigger	—	0.9	2.2
t_{26}	Reference Trigger to POUT	PFI	0.8	2.3
		RTSI	0.8	1.9

Sample Clock

Sample Clock signals the start of a sample (which, in turn, is a set of converts). Sample Clock is generated from external or internal sources. The main internal source is the terminal count (TC) of the SI counter that runs on the Sample Clock Timebase signal. All the sources for Sample Clock are at the _i level and are selected using a multiplexer. The output of this multiplexer is called *Selected Sample Clock*.

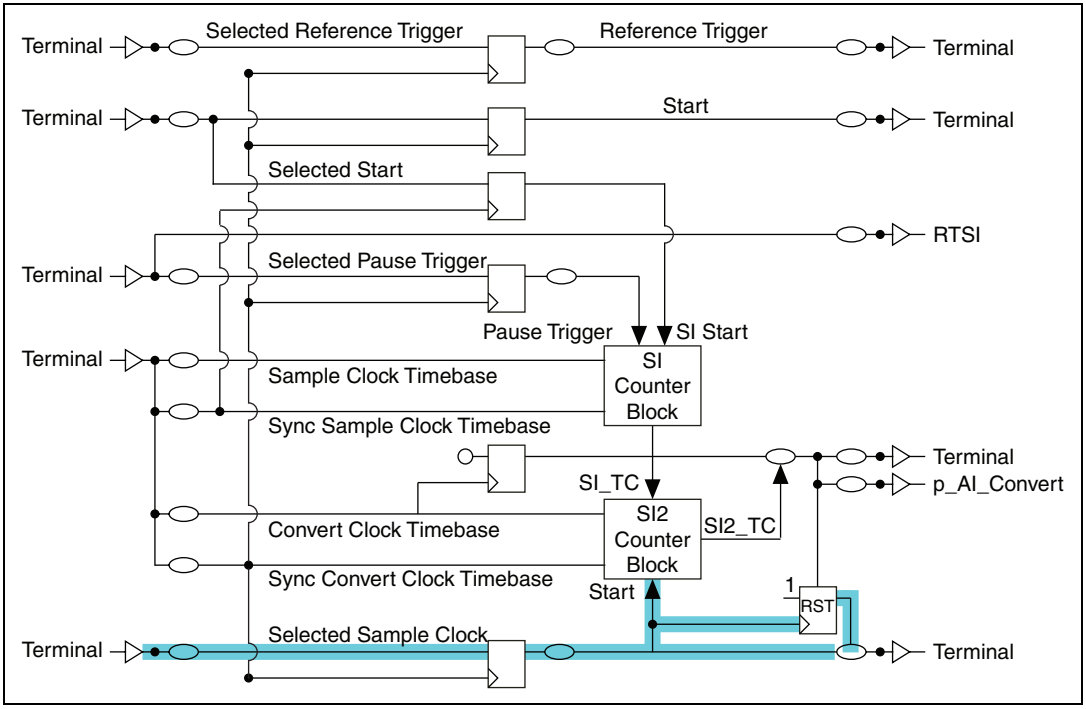

Figure B-15. Sample Clock and the Analog Input Timing Engine

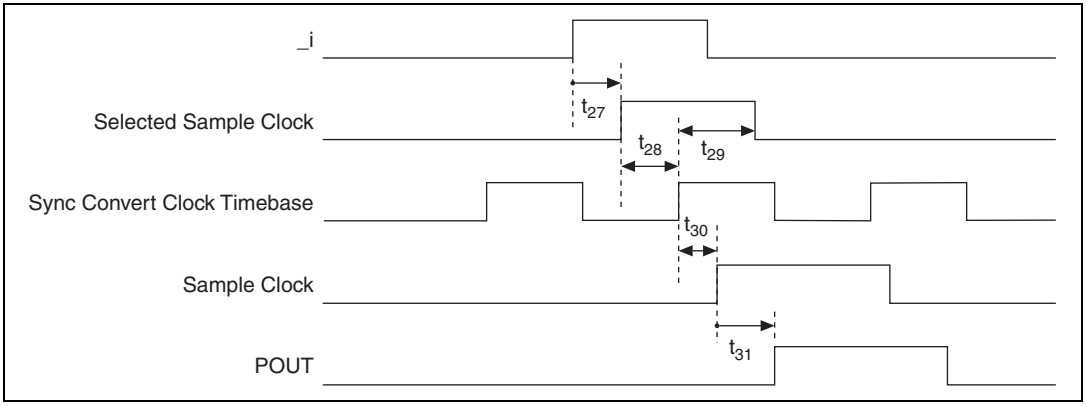

Figure B-16. Sample Clock Timing Diagram

Table B-8. Sample Clock Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{27}	Delay to Selected Sample Clock	PFI	3.5	8.9
		RTSI	3.4	8.6
		STAR	2.8	5.9
t_{28}	Selected Sample Clock Setup time (to Sync Convert Clock Timebase)	—	1.5	—
t_{29}	Selected Sample Clock Hold time (to Sync Convert Clock Timebase)	—	0	—
t_{30}	Sync Convert Clock Timebase to Sample Clock	—	2.4	5.8
t_{31}	Sample Clock to POUT	PFI	2.4	5.5
		RTSI	3.2	6.8

The AI timing engine also can export a signal related to the Sample Clock called AI_Sample_In_Progress. This signal asserts with the Sample Clock and stays asserted until after the last convert of the sample. It is useful for external simultaneous sample and hold signal conditioning.

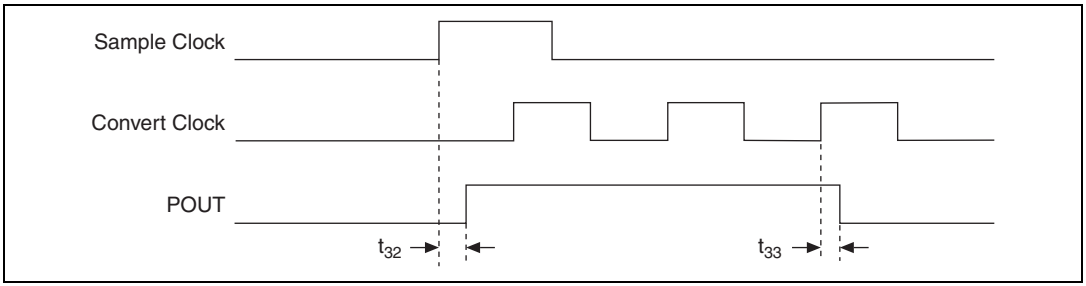

Figure B-17. AI_Sample_In_Progress Timing Diagram

Table B-9. AI_Sample_In_Progress Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{32}	Sample Clock to POUT as leading edge of AI_Sample_In_Progress	PFI	3.4	8.0
		RTSI	4.2	9.2
t_{33}	Convert Clock to POUT as trailing edge of AI_Sample_In_Progress	PFI	5.4	12.4
		RTSI	6.2	13.6

Pause Trigger

The *Pause Trigger* signal can be used to pause the acquisition any time the signal deasserts. It is generated from internal or external sources. A multiplexer selects a signal from the _i bus; its output is called *Selected Pause Trigger.*

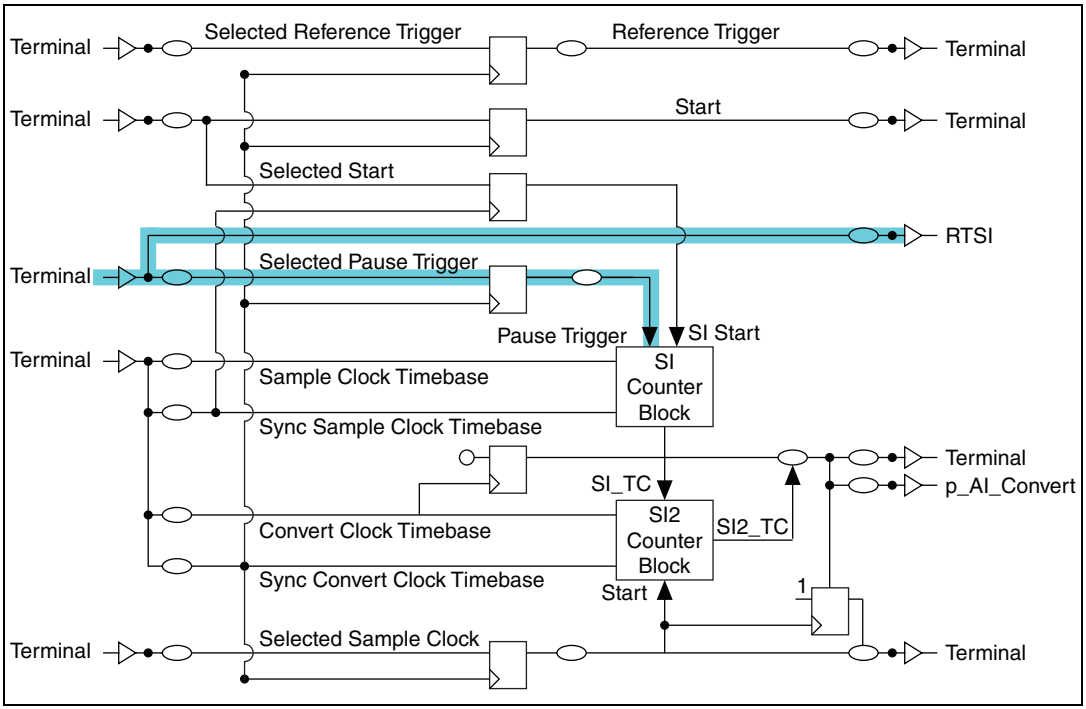

Figure B-18. Pause Trigger and the Analog Input Timing Engine

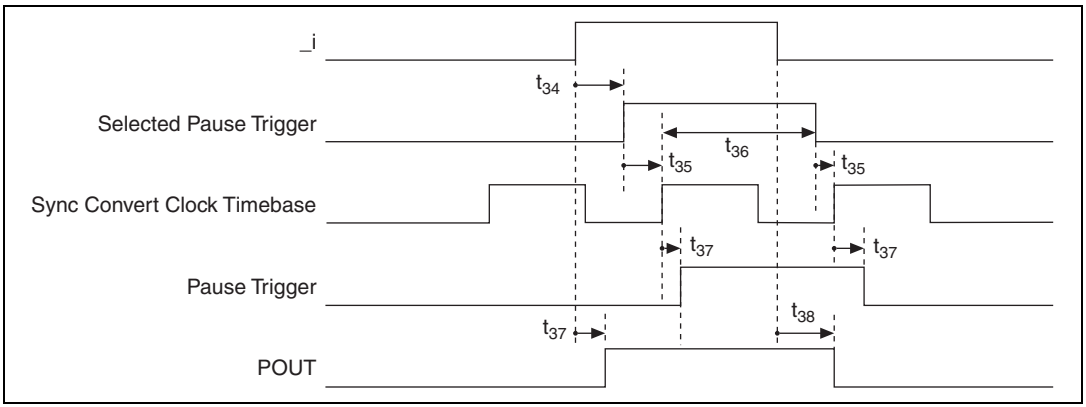

Figure B-19. Pause Trigger Timing Diagram

Table B-10. Pause Trigger Timing

Time	Description	Line	Min (ns)	Max (ns)
t_{34}	_i to Selected Gate	PFI	3.2	7.8
		RTSI	3.0	7.5
		STAR	2.5	4.9
t_{35}	Selected Pause Trigger Setup Time (to Sync Convert Clock Timebase)	—	1.5	—
t_{36}	Hold (Sync Convert Clock Timebase)	—	0	—
t_{37}	Sync Convert Clock Timebase to Pause Trigger	—	0.6	2.6
t_{38}	Pause Trigger Source in _i to POUT	RTSI	1.1	3.1

Output Timing

Output timing refers to the delays involved in exporting internal signals to external terminals, so they can be used to trigger or time external devices. These timing parameters include the selection multiplexer in each terminal plus the delay of the output driver. Figures B-20 and B-21 and Table B-11 describe output timing.

The delays presented in this section assume a 200 pF load on PFI lines and a 50 pF load on RTSI lines. Actual delays will vary with the actual load.

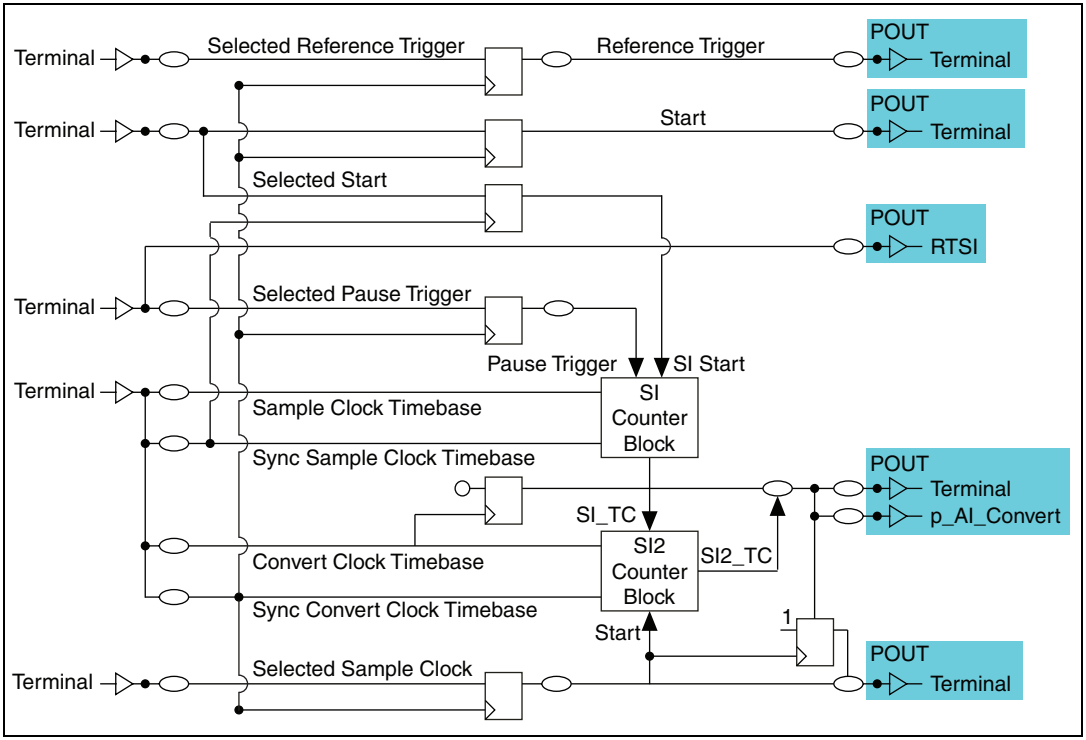

Figure B-20. Output Timing and the Analog Input Timing Engine

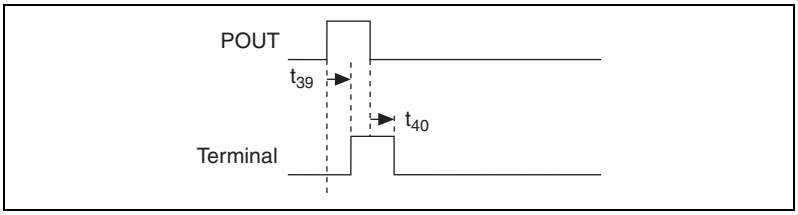

Figure B-21. Output Timing Diagram

Table B-11. Output Timing

Edge	Line	Min (ns)	Max (ns)
Rising Edge	PFI	7.2	25.7
	RTSI	5.6	14.0
Falling Edge	PFI	7.5	25.9
	RTSI	6.0	13.9

Analog Output Timing Diagrams

The analog output timing can be broken into the following three sections:

- *Input Timing*—The timing for external signals to enter the M Series device and be available on the internal signal buses
- *Internal Analog Output Timing*—The timing specifications of the analog output unit itself, to and from internal signals
- *Output Timing*—The timing of exported signals going to the M Series device external terminals

Figure B-22 gives an overview of analog output timing.

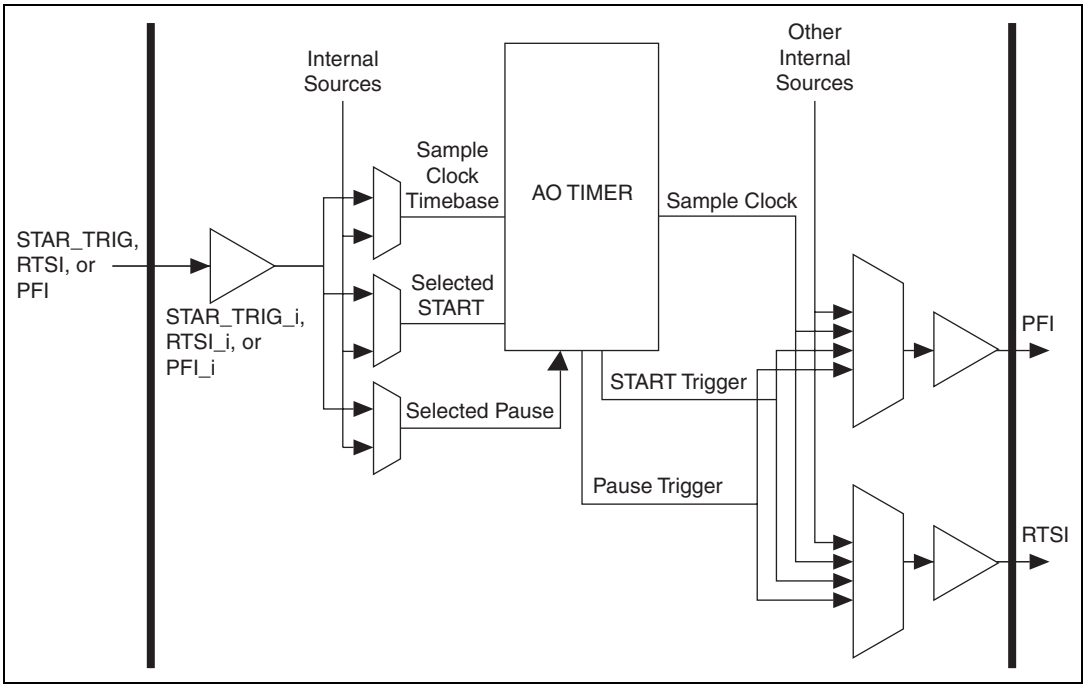

Figure B-22. M Series Analog Output Timing

The following signals are used in Figure B-22 and in the following sections:

- **Sample Clock**—This signal multiplied by the digital to analog conversions. This signal is routed to the DAC, and in every pulse, the DAC will perform a data conversion. This signal can come directly from an external signal or can be the result of dividing down the Sample Clock Timebase using the UI counter.

- **Sample Clock Timebase**—This signal can be used to generate the Sample Clock. This signal acts as the clock for the UI counter, and a Sample Clock can be generated every N periods of the Sample Clock Timebase by programming the UI counter accordingly. This signal can come from an internal source (such as the board oscillator) or an external source.
- **Sync Sample Clock Timebase**—The Sync Sample Clock Timebase is a signal that is generated internally and is related to the Sample Clock Timebase. How it is generated and the relationship between the two signals depends on the mode of operation. In general, the Sync Sample Clock Timebase is used to synchronize the input signals to the analog output timing engine before they are used by the Sample Clock Timebase.
- **Start Trigger, Selected Start**—The Start Trigger determines when a timed analog output operation will start. This signal can come from a software command or an external pulse. Selected Start is the output of the selection block for the Start Trigger source.
- **Pause Trigger, Selected Pause**—The waveform generation can be paused using the pause trigger. When enabled, the waveform generation will occur as long as the gate is enabled. The generation will be paused if the gate is disabled. This signal can come from a software command or an external signal. The Selected Pause is the output of the selection block for the Pause Trigger source.
- **Star_Trig, RTSI, or PFI**—These terminals are the I/O interface for the device. All external triggers are input on these terminals. Internal signals can be exported to these terminals as well.
- **_i Signals**—All signals marked with _i are external signals that have been through the I/O buffers and are ready for internal use.

Input Timing

Input timing refers to the delays of importing signals from the external terminals so that the analog output timing engine can use them as sources for different triggers or clocks. Figure B-23 and Table B-12 describe the insertion delays for external signals.

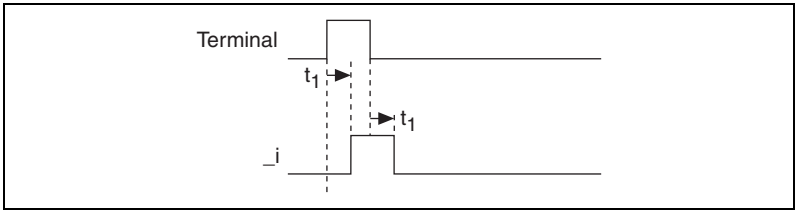

Figure B-23. Input Timing Diagram

Table B-12. Input Timing

Time	From	To	Min (ns)		Max (ns)	
t_1*	PFI	PFI_i	4.1	6.4	15.2	19.2
	RTSI	RTSI_i	0.9	2.2	2.0	3.0
	STAR	STAR_i	0.9	—	—	2.8

* The delay ranges given for PFI and RTSI represent the fastest and slowest terminal routing within the trigger group for a given condition (maximum or minimum timing). This difference can be useful when two external signals will be used together and the relative timing between the signals is important.

Internal Analog Output Timing

The analog output timer has two internal clocks that are referenced—Sample Clock Timebase and Sync Sample Clock Timebase. How they are generated depends on how the analog output timer is configured. If the analog output timing engine is configured to operate with an external Sample Clock, analog output internal clock timing can be derived from Table B-13.

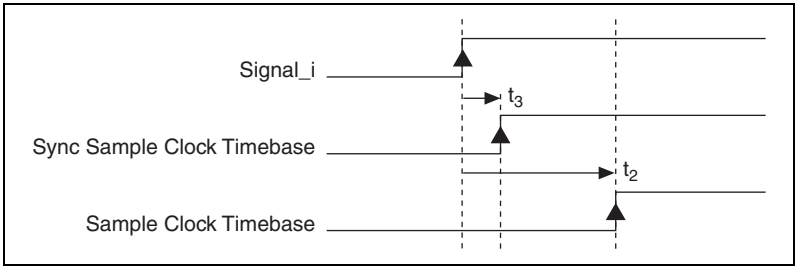

Figure B-24. External Update Source Clock Insertions Timing Diagram

Table B-13. External Update Source Clock Insertions Timing

Time	From	To	Min (ns)	Max (ns)
t_2	Signal_i	Sample Clock Timebase	11.6	30.0
t_3	Signal_i	Sync Sample Clock Timebase	1.5	7.0

If the Sample Clock is being generated by dividing down the Sample Clock Timebase, the analog output generation is timed from the output of the UI counter. The signal Sample Clock Timebase can be an external signal. When the analog output timing engine operates in this mode, it is assumed that the source signal for the Sample Clock timebase is a free-running clock, so the Sync Sample Clock Timebase is the inverted version of Sample Clock Timebase. Configuring the analog output timing engine for rising edge operation will cause the external signals to be synchronized on the falling edge of the Sample Clock Timebase, which corresponds to the rising edge of Sync Sample Clock Timebase.

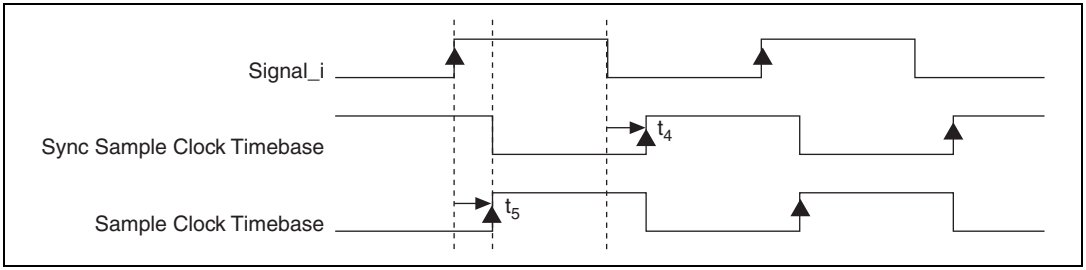

Figure B-25. Sample Clock Timebase and the Sync Sample Clock Timebase Timing Diagram

Table B-14. Sample Clock Timebase and the Sync Sample Clock Timebase Timing

Time	From	To	Min (ns)	Max (ns)
t_4	Signal_i	Sample Clock Timebase	2.4	9.3
t_5	Signal_i	Sync Sample Clock Timebase	2.4	9.3

Start Trigger

As an output, the Start Trigger is routed as an asynchronous pulse. The actual signal that gets routed is the Selected Start signal, so there is no synchronous delay involved.

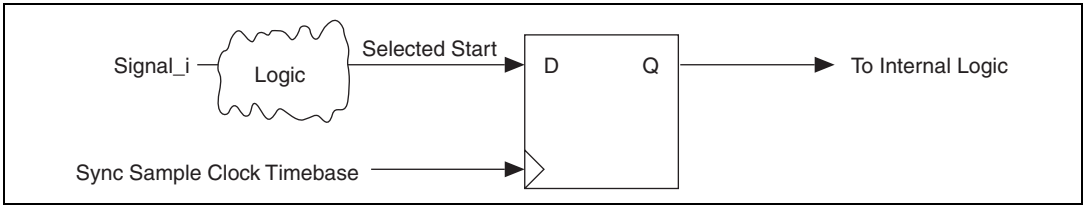

Figure B-26. Start Trigger Input Delay Path

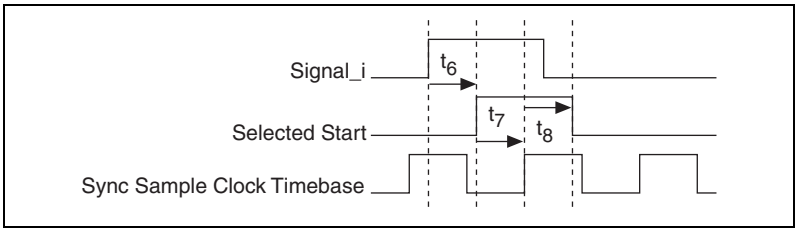

Figure B-27. Start Trigger Timing Diagram

Table B-15. Start Trigger Timing from Signal_i to Selected Start

Time	From	To	Min (ns)	Max (ns)
t_6	Signal_i	Selected Start	2.9	9.8

Table B-16. Start Trigger Setup and Hold Timing

Time	Parameter	Min (ns)	Max (ns)
t_7	Setup	1.5	—
t_8	Hold	0	—

Pause Trigger

The analog output Pause Trigger can be used to pause an ongoing generation. It is received on the rising edge of Sync Sample Clock Timebase.

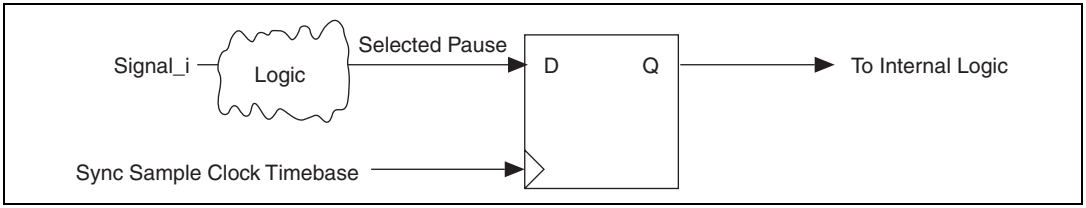

Figure B-28. Pause Trigger Input Delay Path

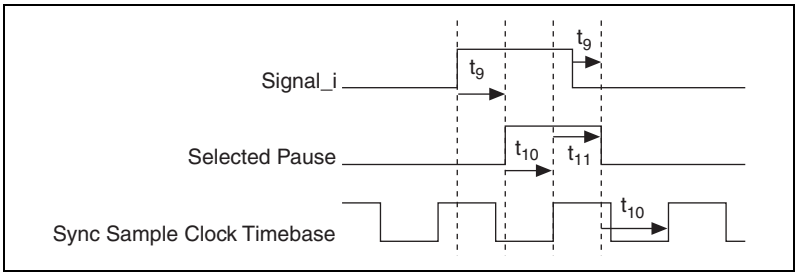

Figure B-29. Pause Trigger Timing Diagram

Table B-17. Pause Trigger Timing from Signal_i to Selected Pause

Time	From	To	Min (ns)	Max (ns)
t_9	Signal_i	Selected Pause	1.7	7.8

Table B-18. Pause Trigger Setup and Hold Timing

Time	Parameter	Min (ns)	Max (ns)
t_{10}	Setup	1.5	—
t_{11}	Hold	0	—

Input Timing Verification

Consider an application that uses an external trigger and an external clock. The trigger and clock signals are routed to an internal D flip-flop (DFF). To ensure that the trigger is sampled on a particular clock edge, the setup and hold times of the internal DFF must be met:

- Recall that a “terminal” is a PFI pin, RTSI pin, or PXI_Star pin.
- Let TriggerDelay be the delay from the trigger terminal to the DFF.
- Let ClockDelay be the delay from the clock terminal to the DFF.

- Let DFF_{Setup} and DFF_{Hold} be the setup and hold time of the DFF.
- Let $External_{Setup}$ and $External_{Hold}$ be the setup and hold time of the trigger to the clock at the terminals.

Figure B-30 shows the external trigger and external clock and the trigger delay and clock delay.

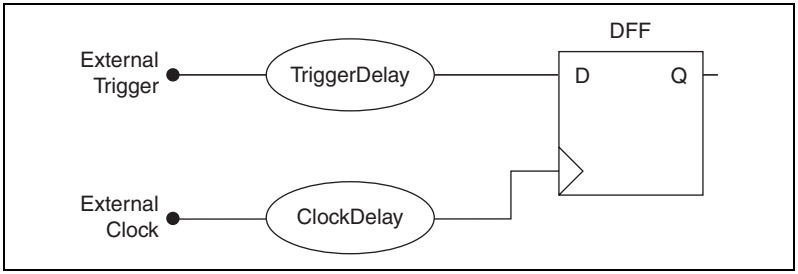

Figure B-30. External Trigger and External Clock Application

To satisfy the DFF setup and hold requirement, the following condition must be true:

$$External_{Setup} \geq DFF_{Setup} - ClockDelay + TriggerDelay$$

$$External_{Hold} \geq DFF_{Hold} + ClockDelay - TriggerDelay$$

DFF_{Setup} and DFF_{Hold} are given by Table B-16 for AO Start and Table B-18 for AO Pause triggers.

ClockDelay is the sum of the input timing (shown in Table B-12), and insertion timing (shown in Table B-13).

TriggerDelay is the sum of the input timing (shown in Table B-12), and internal timing (shown in Tables B-15 and B-17).

For setup calculations, use the maximum timing parameters. For hold calculations, use the minimum timing parameters.

For input timing, as shown in Table B-12, two numbers are given for the maximum delay and two numbers for the minimum delay. In order to account for the worst case skew between different input terminals, use the range given in the input delay tables in the *Input Timing* section in a way that provides the most conservative results. For setup calculations, use the bigger number for TriggerDelay and the smaller number ClockDelay. For hold calculations, use the smaller number for TriggerDelay and the larger number for ClockDelay.

Output Timing

The analog output timer has three possible trigger outputs—Start Trigger, Pause Trigger, and Sample Clock. The delays presented in this section assume a 200 pF load on PFI lines and a 50 pF load on RTSI lines. Actual delays will vary with the actual load. The two numbers given for each condition represent the variation from the best case and worst case terminals.

Start Trigger

As an output, the Start Trigger is routed as an asynchronous pulse. The actual signal that gets routed is the Selected Start signal, so there is no synchronous delay involved.

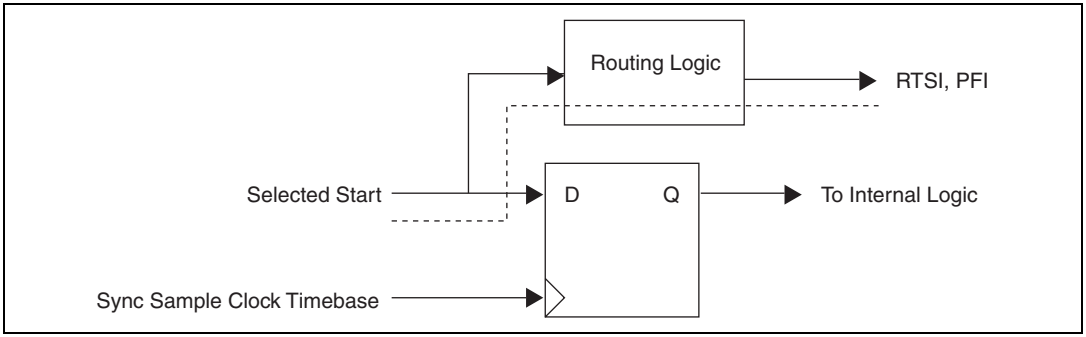

Figure B-31. Start Trigger Path

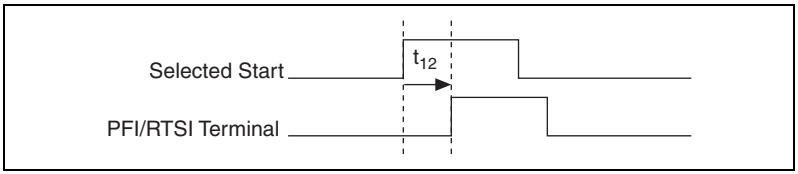

Figure B-32. Start Trigger Output Delay Timing Diagram

Table B-19. Start Trigger Output Delay Timing

Time	From	To	Min (ns)		Max (ns)	
t_{12}	Selected Start	PFI	8.1	9.1	27.1	30.8
	Selected Start	RTSI	7.5	7.7	17.9	18.5

Pause Trigger

Pause Trigger is only output asynchronously and only to RTSI. The actual signal being routed is Selected Pause. The Pause Trigger output timing can be derived by adding the delay in Table B-20 to the total Selected Pause delay.

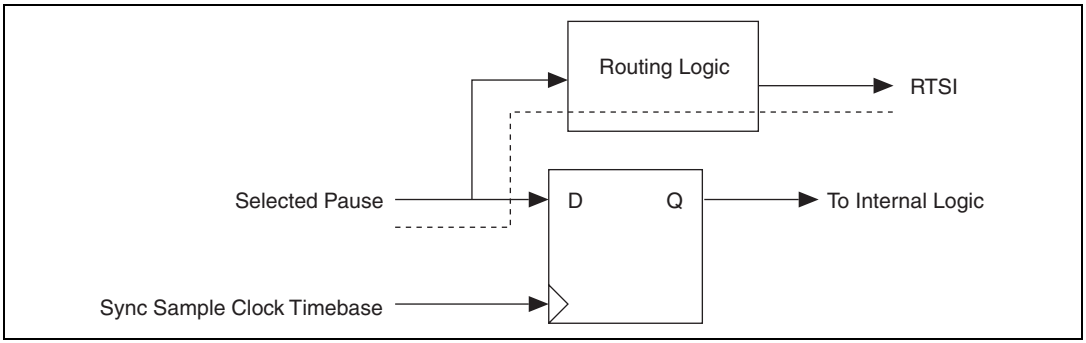

Figure B-33. Pause Trigger Path

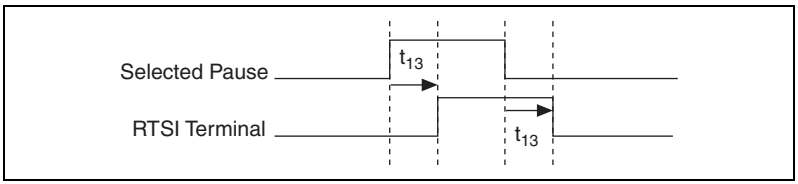

Figure B-34. Pause Trigger Output Routing Delay Timing Diagram

Table B-20. Pause Trigger Output Routing Delay Timing

Time	From	To	Min (ns)		Max (ns)	
t_{13}	Selected Pause	RTSI	6.7	7.1	16.3	17.0

Sample Clock

The rising edge of the Sample Clock is output synchronous to the Sample Clock Timebase. It can be calculated by adding the Sample Clock Timebase insertion to the delay in Table B-21. The exported Sample Clock signal is active low, each falling edge representing a conversion.

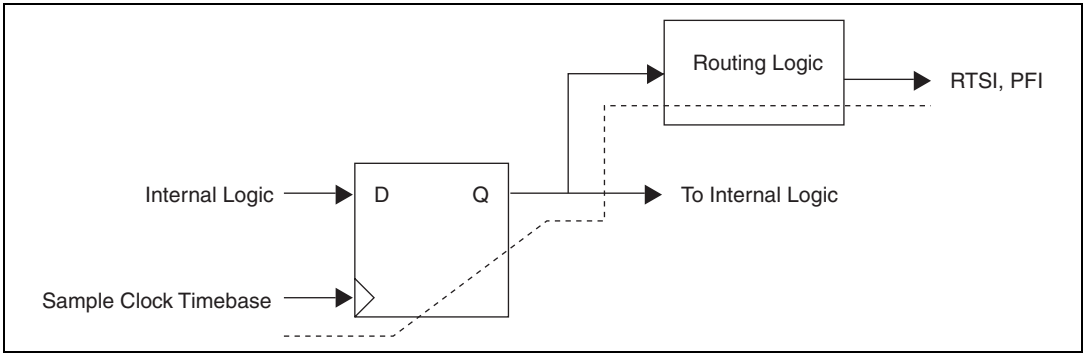

Figure B-35. Sample Clock Path

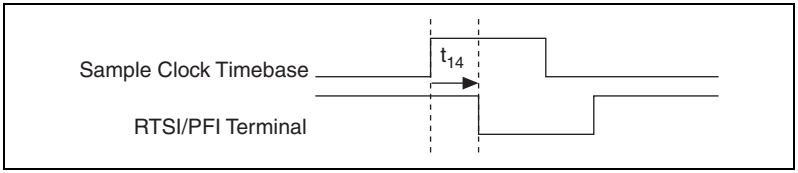

Figure B-36. Sample Clock Delay Timing Diagram

Table B-21. Sample Clock Delay Timing

Time	From	To	Min (ns)		Max (ns)	
t_{14}	AO Sample Clock	PFI	9.7	10.7	31.1	34.3
	AO Sample Clock	RTSI	8.8	9.1	21.3	21.7

Digital I/O Timing Diagrams

This section describes the timing delays and requirements of digital waveform acquisitions and digital waveform generations.

Digital Waveform Acquisition Timing

To describe digital waveform acquisition timing delays and requirements, refer to the circuitry shown in Figure B-37. In the figure, P0, PFI, RTSI, and PXI_STAR represent signals at connector pins of the M Series device. The other named signals represent internal signals.

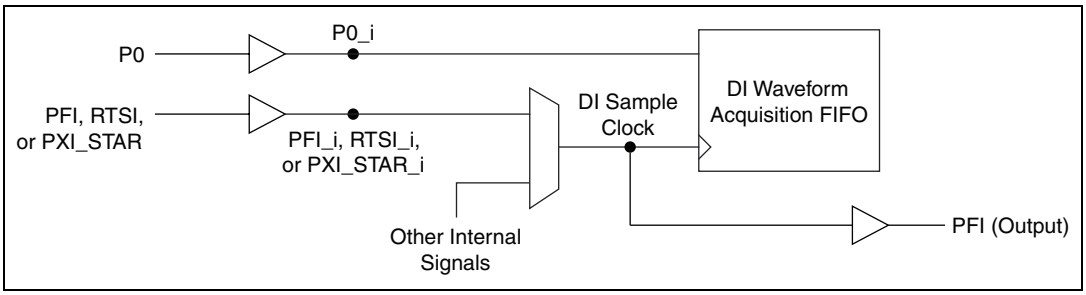

Figure B-37. Digital Waveform Acquisition Timing Circuitry

Figure B-38 and Tables B-22 and B-23 describe the digital waveform acquisition timing delays and requirements. Your inputs must meet the requirements to ensure proper behavior.

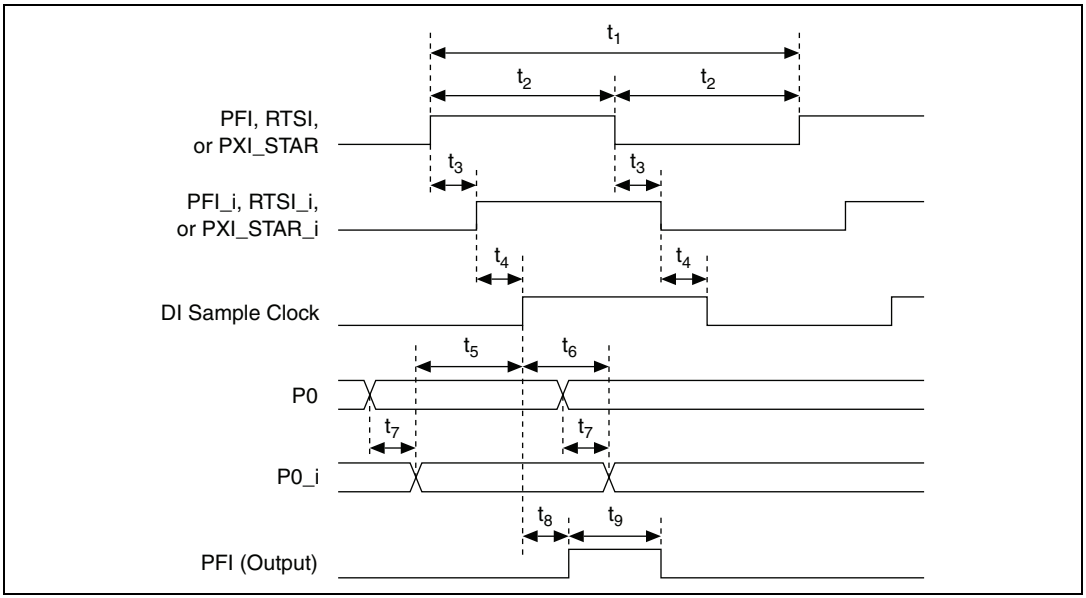

Figure B-38. Digital Waveform Acquisition Timing Delays

Table B-22. DI Timing Delays

Time	From	To	Min (ns)		Max (ns)	
t_3*	PFI	PFI_i	5.2	6.2	18.2	22.0
	RTSI	RTSI_i	2.0	2.5	5.0	6.0
	PXI_STAR	PXI_STAR_i	1.5		3.5	
t_4	PFI_i, RTSI_i, PXI_STAR_i, or other internal signal	DI Sample Clock	3.5		9	
t_7	P0	P0_i	4.7		20.1	
t_8	DI Sample Clock	PFI (output)	8.0		29.8	
t_9†	PFI (output) high	PFI (output) low	One period of 80 MHz Timebase		Two periods of 80 MHz Timebase	

* The delay ranges given for PFI and RTSI represent the fastest and slowest terminal routing within the trigger group for a given condition (maximum or minimum timing). This difference can be useful when two external signals will be used together and the relative timing between the signals is important.

† When DI Sample Clock is routed to a PFI output pin, the pulse width of the output is independent of the pulse width of the input. The pulse width is specified in a number of periods of the 80 MHz Timebase

Table B-23. DI Timing Requirements

Time	Requirement	Condition	Min (ns)	Max (ns)
t_1	PFI, RTSI, or PXI_STAR Minimum Period	When used as DI Sample Clock	NI 622*x* devices: 1000.0 NI 625*x*/628*x* devices: 100.0	—
t_2	PFI, RTSI, or PXI_STAR Minimum Pulse Width	When used as DI Sample Clock	12.0	—
t_5	Setup time From P0_i to DI Sample Clock	—	1.5	—
t_6	Hold time From DI Sample Clock to P0_i	—	0	—

Digital Waveform Generation Timing

To describe digital waveform generation timing delays and requirements, we model the circuitry as shown in Figure B-39. In the figure, P0, PFI, RTSI, and PXI_STAR represent signals at connector pins of the M Series device. The other named signals represent internal signals.

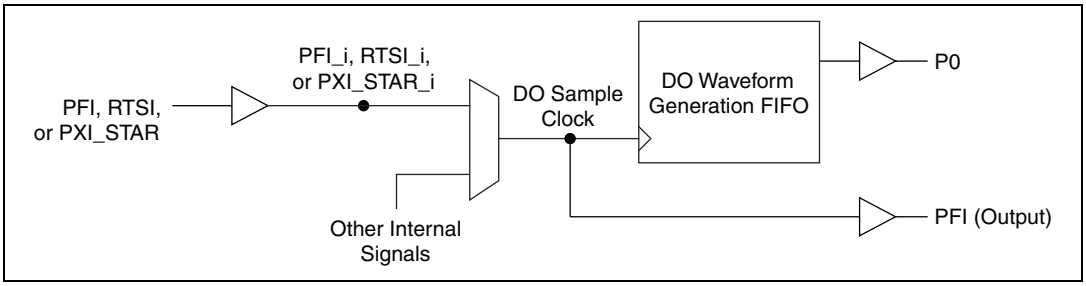

Figure B-39. Digital Waveform Generation Timing Circuitry

Figure B-40 and Tables B-24 and B-25 describe the digital waveform generation timing delays and requirements. Your inputs must meet the requirements to ensure proper behavior.

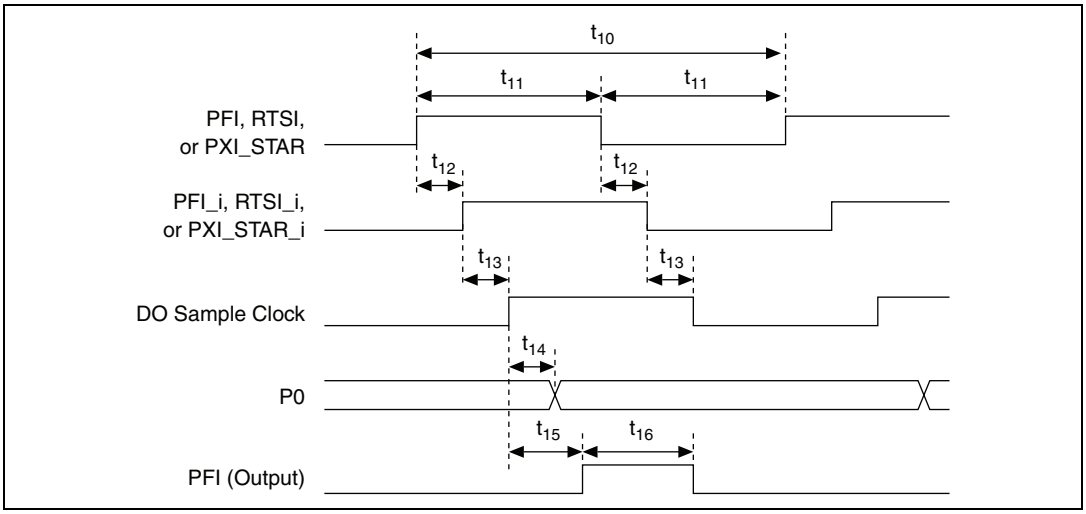

Figure B-40. Digital Waveform Acquisition Timing Delays

Table B-24. DO Timing Delays

Time	From	To	Min (ns)		Max (ns)	
t_{12}*	PFI	PFI_i	5.2	6.2	18.2	22.0
	RTSI	RTSI_i	2.0	2.5	5.0	6.0
	PXI_STAR	PXI_STAR_i	1.5		3.5	
t_{13}	PFI_i, RTSI_i, PXI_STAR_i, or other internal signal	DO Sample Clock	3.5		9.5	
t_{14}	DO Sample Clock	P0	7.5		27.5	
t_{15}	DO Sample Clock	PFI (output)	8.0		29.8	
t_{16}†	PFI (output) high	PFI (output) low	Two periods of 80 MHz Timebase		Three periods of 80 MHz Timebase	

* The delay ranges given for PFI and RTSI represent the fastest and slowest terminal routing within the trigger group for a given condition (maximum or minimum timing). This difference can be useful when two external signals will be used together and the relative timing between the signals is important.

† When DO Sample Clock is routed to a PFI output pin, the pulse width of the output is independent of the pulse width of the input. The pulse width is specified in a number of periods of the 80 MHz Timebase.

Table B-25. DO Timing Requirements

Time	Requirement	Condition	Min (ms)	Max (ms)
t_{10}	PFI, RTSI, or PXI_STAR Minimum Period	When used as DO Sample Clock	NI 622*x* devices: 1000.0 NI 625*x*/NI 628*x* devices: 100.0	—
t_{11}	PFI, RTSI, or PXI_STAR Minimum Pulse Width	When used as DO Sample Clock	12.0	—

Counters Timing Diagrams

This section describes input delays, input requirements, output delays, gating modes, and quadrature and two pulse encoder timing.

Input Delays

This section describes some of the timing delays of the counter/timer circuit. To describe delays of the counter/timer, we model the circuitry as shown in Figure B-41. In the figure, PFI, RTSI, and PXI_STAR represent signals at connectors pins of the M Series device. The other named signals represent internal signals.

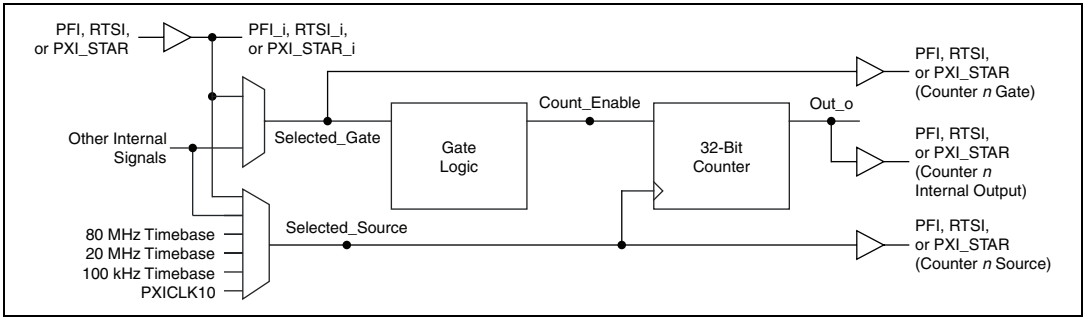

Figure B-41. Counter/Timer Circuitry

Pin to Internal Signal Delays

Input timing is the timing specification for importing a signal to an internal bus on the M Series device. Table B-26 shows the input timing for the counters on all input terminals. Signals refer to the signal at the I/O connector of the device, and signals appended with _i refer to the signal internal to the device after the input buffer.

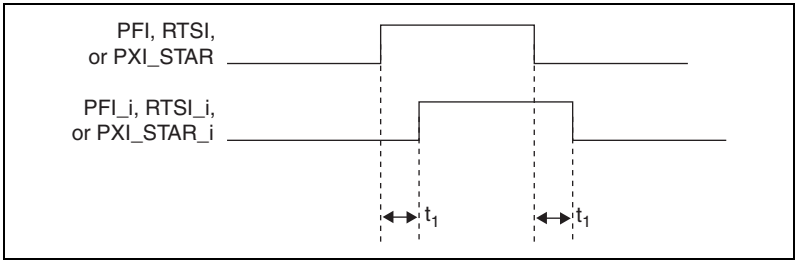

Figure B-42. Pin to Internal Signal Delays Timing Diagram

Table B-26. Pin to Internal Signal Delays Timing

Time	From	To	Min (ns)		Max (ns)	
t_1*	PFI	PFI_i	5.2	6.2	18.2	22.0
	RTSI	RTSI_i	2.0	2.5	5.0	6.0
	STAR	STAR_i	0.9	—	—	2.5

* The delay ranges given for PFI and RTSI represent the fastest and slowest terminal routing within the trigger group for a given condition (maximum or minimum timing). This difference can be useful when two external signals will be used together and the relative timing between the signals is important.

Selected Gate and Selected Source Delays

Tables B-27 and B-28 show the timing for the Selected Source and Selected Gate internal signals.

Selected Source is used to clock the 32-bit counter. Selected Gate drives the Gate Logic, which generates the Counter Enable signal.

All internal counter timing is referenced to these two signals. Any internal signal refers to signals with _i from the previous table or signals coming from another subsystem inside the M Series device. It does not include internal timebases or the PXI_CLK10.

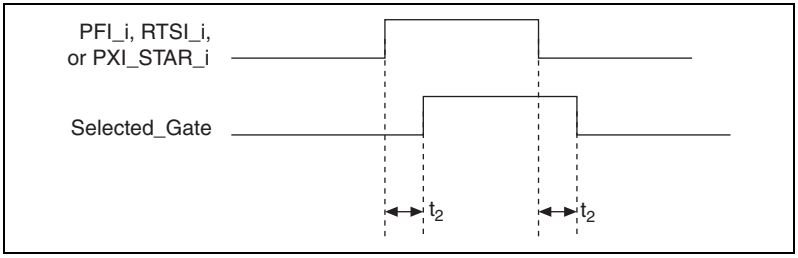

Figure B-43. Selected Gate Delays Timing Diagram

Table B-27. Selected Gate Delays Timing

Time	From	To	Min (ns)	Max (ns)
t_2	PFI_i, RTSI_i, PXI_STAR_i, or any internal signal	Selected Gate	1.0	6.0

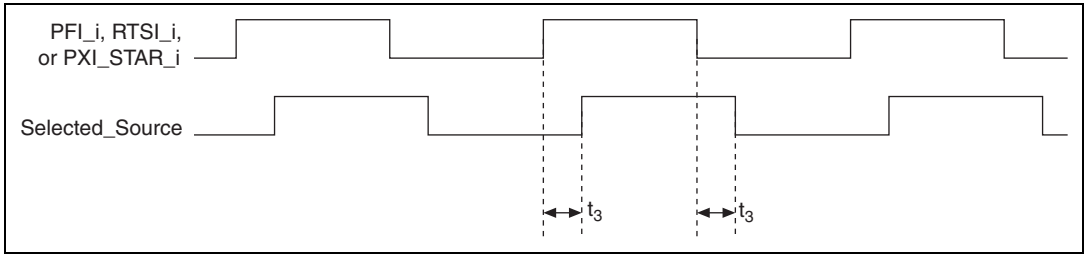

Figure B-44. Selected Source Delays Timing Diagram

Table B-28. Selected Source Delays Timing

Time	From	To	Min (ns)	Max (ns)
t_3	PFI_i, RTSI_i, PXI_STAR_i, or any internal signal	Selected Source	8.0	21.0
	20 MHz Timebase	Selected Source	1.5	4.0
	100 kHz Timebase	Selected Source	1.5	4.0
	80 MHz Timebase	Selected Source	1.0	2.5
	PXI_CLK10	Selected Source	1.0	3.5

Count Enable Delay

Table B-29 shows timing for the internal Count Enable signal, as shown in Figure B-41. Count Enable enables the 32-bit counter to count on the rising edge of the Selected Source signal.

The delays depend on both the synchronization mode and gating mode for the application.

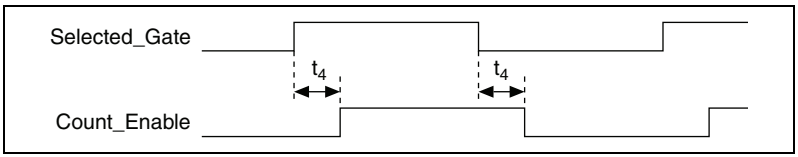

Figure B-45. Count Enable Delays

Table B-29. Selected Gate to Count Enable Delays

Time	Synchronization Mode	Gating Mode	Min (ns)	Max (ns)
t_4	80 MHz Source	Edge	0.5	5.0
		Level	–1.0	0.5
	Other Internal Source	Edge	1/2 Source Period – 1 ns	1/2 Source Period + 3 ns
		Level	1/2 Source Period – 2.5 ns	1/2 Source Period – 1 ns
	External Source	Edge	7.5	22.0
		Level	6.0	18.0

Input Requirements

Refer to the Figure B-41 for the M Series counter/timer circuitry.

Source Period and Pulse Width

Figure B-46 and Table B-30 show the timing requirements for Counter *n* Source. The requirements depend on the synchronization mode.

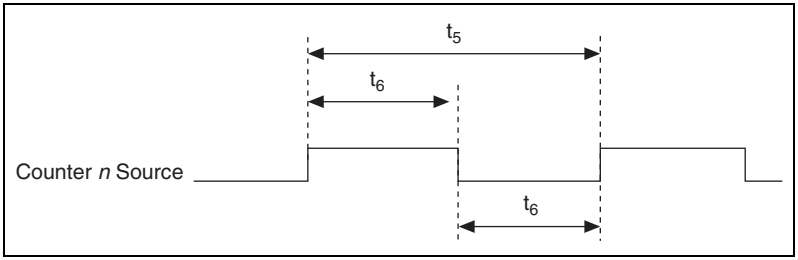

Figure B-46. Counter *n* Source Timing Requirements

Table B-30. Counter *n* Source Timing

Time	Description	Synchronization Mode	Min (ns)*	Max (ns)
t_5	Counter *n* Source Period	80 MHz Source	12.5	—
		Other Internal Source	25.0	—
		External Source	50.0	—
t_6	Counter *n* Source Pulse Width	80 MHz Source	6.2	—
		Other Internal Source	12.5	—
		External Source	16.0	—

* The times in this table are measured at the pin of the M Series device. For example, t_5 specifies the minimum period of a signal driving a PFI, RTSI, or PXI_STAR pin when that signal is internally routed to Counter *n* Source.

Gate Pulse Width

Figure B-47 and Table B-31 show the timing requirements for Counter *n* Gate. The requirements depend on the gating mode.

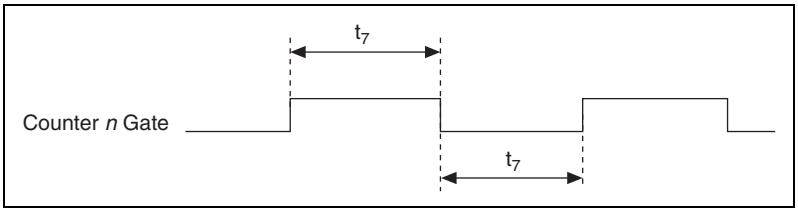

Figure B-47. Counter *n* Gate Pulse Width Timing Diagram

Table B-31. Counter *n* Gate Pulse Width Timing

Time	Description	Gating Mode	Min (ns)*	Max (ns)
t_7	Counter *n* Gate Pulse Width	Edge	12.0	—
	Counter *n* Gate Pulse Width	Level	One Source Period	—

* The times in this table are measured at the pin of the M Series device. That is, t_7 specifies the minimum pulse width of a signal driving a PFI, RTSI, or PXI_STAR pin when that signal is internally routed to Counter *n* Gate.

Gate to Source Setup and Hold

The counter can be modeled as a set of flip flops where the D input is Count Enable and the clock input is Selected Source, as shown in Figure B-41. This section shows the setup and hold requirements for two different cases:

- A PFI pin drives Counter *n* Source and a different PFI pin drives Counter *n* Gate
- The general case (all other combinations of signals driving Source and Gate)

Figure B-48 and Table B-32 show the setup and hold requirements at the PFI pins for the first case (where a PFI pin drives Counter *n* Source and a different PFI pin drives Counter *n* Gate).

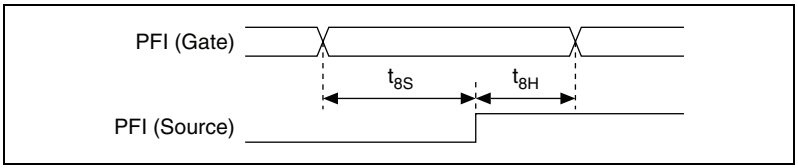

Figure B-48. Gate to Source Setup and Hold Timing Diagram

Table B-32. Gate to Source Setup and Hold Timing

Time	Description	Gating Mode	Synchronization Mode	Min (ns)	Max (ns)
t_{8S}	Setup time from PFI (Gate) to PFI (Source)	Edge	External Source	12.3	—
		Level	External Source	8.3	—
t_{8H}	Hold time from PFI (Gate) to PFI (Source)	Edge	External Source	0.5	—
		Level	External Source	2.0	—

Figure B-49 and Table B-33 show the setup and hold requirements of the internal block of the DAQ-STC2. Use the table to calculate the setup and hold times for your Source and Gate signals for the general case. In the general case, you can determine whether the setup and hold requirements are met by adding up the various delays of the appropriate signals through the counter/timer circuit.

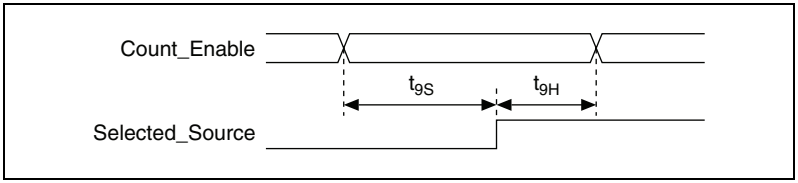

Figure B-49. DAQ-STC2 Internal Block Setup and Hold Requirements Timing Diagram

Table B-33. DAQ-STC2 Internal Block Setup and Hold Requirements Timing

Time	Parameter	Min (ns)	Max (ns)
t_{9S}	Setup	1.5	—
t_{9H}	Hold	0	—

Example of the General Case

Calculate the setup and hold time requirements when the Gate and Source come from PFI lines and the Gate is used in level mode.

Note This example shows how we determine the setup and hold times for the PFI to PFI example above (first case) using level gating.

Setup

To calculate the setup time, subtract the Source delay from the Gate delay. Use maximum delays.

Gate Delay

PFI to PFI_i	22.0 ns
PFI_i to Selected Gate	6.0 ns
Selected Gate to Count Enable (Level)	18.0 ns
Count Enable Setup Time	+ 1.5 ns
	47.5 ns

Source Delay

PFI to PFI_i	18.2 ns
PFI_i to Selected Source	+ 21.0 ns
	39.2 ns

$T_{Setup} > 47.5 \text{ ns} - 39.2 \text{ ns} = 8.3 \text{ ns}$

Hold

To calculate the hold time, subtract the Gate delay from the Source delay. Use minimum delays.

Gate Delay

PFI to PFI_i	5.2 ns
PFI_i to Selected Gate	1.0 ns
Selected Gate to Count Enable (Level)	6.0 ns
Count Enable Hold Time	+ 0.0 ns
	12.2 ns

Source Delay

PFI to PFI_i	6.2 ns
PFI_i to Selected Source	+ 8.0 ns
	14.2 ns

$T_{Hold} > 14.2 \text{ ns} - 12.2 \text{ ns} = 2.0 \text{ ns}$

Output Delays

Refer to the Figure B-41 for the M Series counter/timer circuitry.

Figure B-50 and Table B-34 show the output delays.

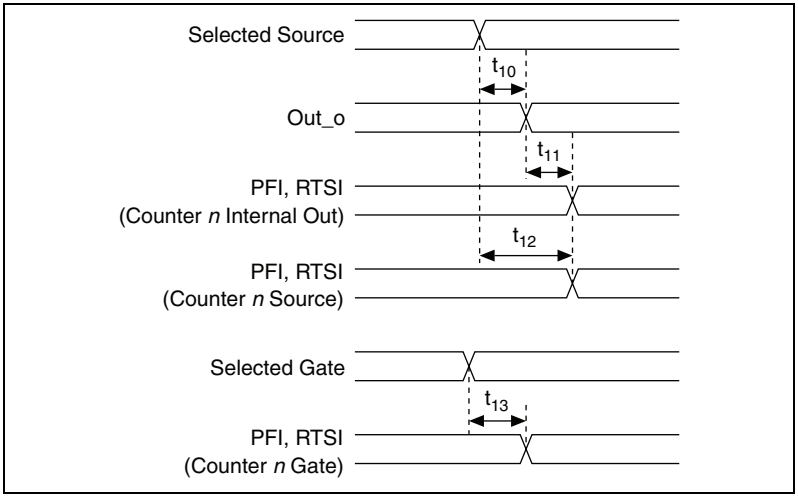

Figure B-50. Output Delays

Table B-34. Output Delays Timing

Time	Line	Min (ns)	Max (ns)
t_{10}	—	1.0	4.0
t_{11}	PFI	7.5	28.2
	RTSI	6.5	18.0
t_{12}	PFI	8.5	32.2
	RTSI	7.5	22.0
t_{13}	PFI	7.5	28.7
	RTSI	6.5	18.0

Gating Modes

Gating mode refers to how the counter/timer uses the Gate input. Some timing operations depend on the gating mode. Depending on the application, the counter/timers either level gating mode or edge gating mode.

In NI-DAQmx, the counter/timers use level gating mode for the following measurements:

- Edge counting
- Pulse width measurements
- Two-signal edge separation measurements

All other measurements use edge gating mode.

Quadrature and Two Pulse Encoder Timing

Counter *n* A, Counter *n* B, and Counter *n* Z, described in the *Counter n A, Counter n B, and Counter n Z Signals* section of Chapter 7, *Counters*, are used in position measurements using quadrature encoder or two-pulse encoder counting modes. Table B-35 shows the timing requirements for these signals.

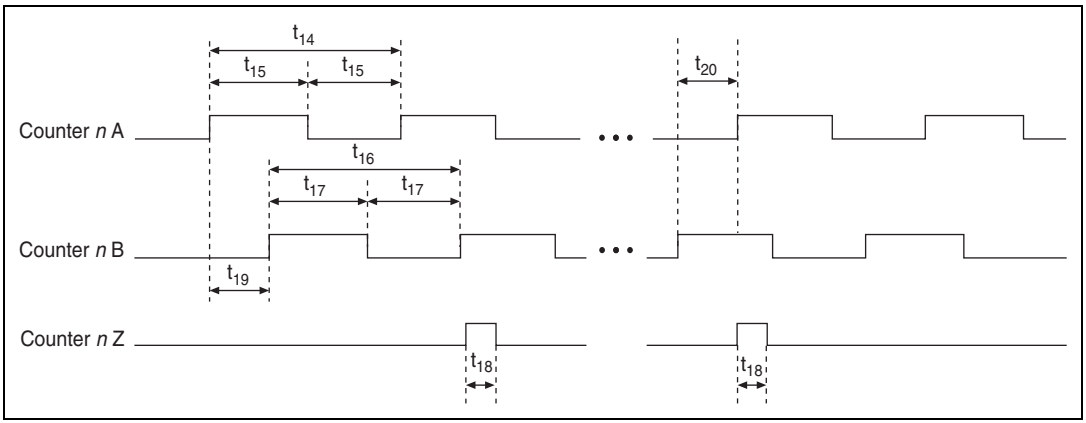

Figure B-51. Quadrature and Two Pulse Encoder Timing Diagrams

Table B-35. Quadrature and Two Pulse Encoder Timing

Time	Description	Min (ns)*	Max (ns)
t_{14}	Counter *n* A Period	50.0	—
t_{15}	Counter *n* A Pulse Width	25.0	—
t_{16}	Counter *n* B Period	50.0	—
t_{17}	Counter *n* B Pulse Width	25.0	—
t_{18}	Counter *n* Z Pulse Width	25.0	—
t_{19}	Delay from Counter *n* A to Counter *n* B	25.0	—
t_{20}	Delay from Counter *n* B to Counter *n* A	25.0	—

* The times in this table are measured at the pin of the M Series device. For example, t_{14} specifies the minimum period of a signal driving a PFI, RTSI, or PXI_STAR pin when that signal is internally routed to Counter *n* A.

Clock Generation Timing Diagrams

Table B-36 shows delays for generating different clocks, described in the *Clock Routing* section of Chapter 9, *Digital Routing and Clock Generation*, from the onboard 80 MHz oscillator.

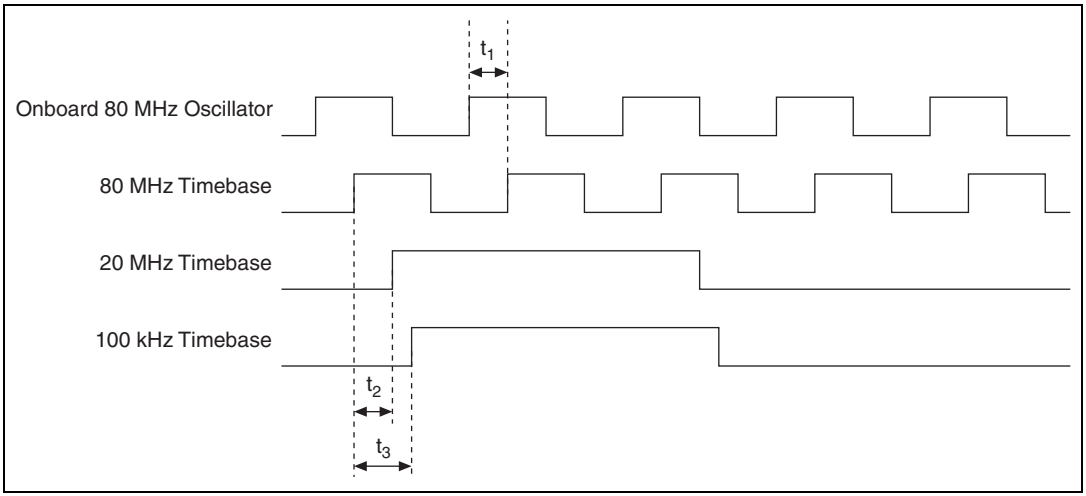

Figure B-52. Generating Different Clocks from the Onboard 80 MHz Oscillator

Table B-36. Generating Different Clocks from the Onboard 80 MHz Oscillator

Time	From	To	Min (ns)	Max (ns)
t_1	Onboard 80 MHz Oscillator	80 MHz Timebase	4.0	9.0
t_2	80 MHz Timebase	20 MHz Timebase	0.5	2.5
t_3	80 MHz Timebase	100 kHz Timebase	1.0	5.0

Table B-37 shows delays for generating different clocks using an External Reference Clock and the PLL.

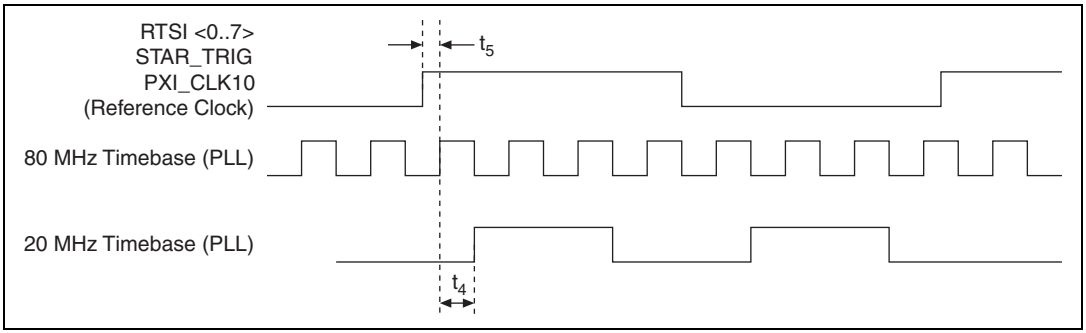

Figure B-53. Generating Different Clocks Using an External Reference Clock and the PLL

Table B-37. Generating Different Clocks Using an External Reference Clock and the PLL

Time	From	To	Min (ns)	Max (ns)
t_4	80 MHz Timebase	20 MHz Timebase	1.5	5.0
t_5	The source of the external reference clock (RTSI <0..7>, STAR_TRIG, PXI_CLK10)	80 MHz Timebase (through PLL_OUT)	1.0	5.5

C

Troubleshooting

This section contains common questions about M Series devices. If your questions are not answered here, refer to the National Instruments KnowledgeBase at `ni.com/kb`.

Analog Input

I am seeing crosstalk or ghost voltages when sampling multiple channels. What does this mean?

You may be experiencing a phenomenon called *charge injection*, which occurs when you sample a series of high-output impedance sources with a multiplexer. Multiplexers contain switches, usually made of switched capacitors. When a channel, for example AI 0, is selected in a multiplexer, those capacitors accumulate charge. When the next channel, for example AI 1, is selected, the accumulated current (or charge) leaks backward through channel 1. If the output impedance of the source connected to AI 1 is high enough, the resulting reading can somewhat affect the voltage in AI 0. To circumvent this problem, use a voltage follower that has operational amplifiers (op-amps) with unity gain for each high-impedance source before connecting to an M Series device. Otherwise, you must decrease the sample rate for each channel.

Another common cause of channel crosstalk is due to sampling among multiple channels at various gains. In this situation, the settling times can increase. For more information about charge injection and sampling channels at different gains, refer to the *Multichannel Scanning Considerations* section of Chapter 4, *Analog Input*.

I am using my device in differential analog input ground-reference mode and I have connected a differential input signal, but my readings are random and drift rapidly. What is wrong?

In DIFF mode, if the readings from the DAQ device are random and drift rapidly, you should check the ground-reference connections. The signal can be referenced to a level that is considered floating with reference to the device ground reference. Even if you are in DIFF mode, you must still reference the signal to the same ground level as the device reference. There

are various methods of achieving this reference while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in the *Connecting Analog Input Signals* section of Chapter 4, *Analog Input*.

AI GND is an AI common signal that routes directly to the ground connection point on the devices. You can use this signal if you need a general analog ground connection point to the device. Refer to the *When to Use Differential Connections with Ground-Referenced Signal Sources* section of Chapter 4, *Analog Input*, for more information.

How can I use the AI Sample Clock and AI Convert Clock signals on an M Series device to sample the AI channel(s)?

M Series devices use ai/SampleClock and ai/ConvertClock to perform interval sampling. As Figure C-1 shows, ai/SampleClock controls the sample period, which is determined by the following equation:

1/sample period = sample rate

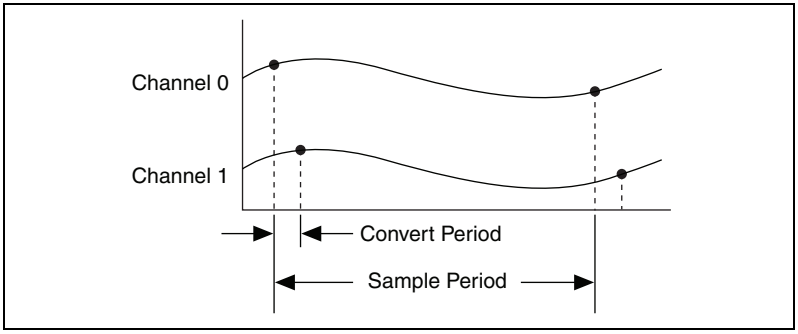

Figure C-1. ai/SampleClock and ai/ConvertClock

ai/ConvertClock controls the convert period, which is determined by the following equation:

1/convert period = convert rate

This method allows multiple channels to be sampled relatively quickly in relationship to the overall sample rate, providing a nearly simultaneous effect with a fixed delay between channels.

Analog Output

I am seeing glitches on the output signal. How can I minimize it?

When you use a DAC to generate a waveform, you may observe glitches on the output signal. These glitches are normal; when a DAC switches from one voltage to another, it produces glitches due to released charges. The largest glitches occur when the most significant bit of the DAC code changes. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of the output signal. Visit `ni.com/support` for more information about minimizing glitches.

Counters

When multiple sample clocks on my buffered counter measurement occur before consecutive edges on my source, I see weird behavior. Why?

Duplicate count prevention ensures that the counter returns correct data for counter measurement in some applications where a slow or non-periodic external source is used.

Refer to the *Duplicate Count Prevention* section of Chapter 7, *Counters*, for more information.

How do I connect counter signals to my M Series device?

The *Default Counter/Timer Pinouts* section of Chapter 7, *Counters*, has information about counter signal connections.

M Series Installation Issues

My M Series device is not detected by Measurement & Automation Explorer (MAX) or the Windows 2000/NT/XP operating system. When using other devices (such as E Series devices) on the same PC, they work fine. What is the problem?

Appendix D, *Upgrading from E Series to M Series*, lists issues encountered when upgrading from E Series to M Series devices.

Customers also can refer to NI's KnowledgeBase at `ni.com/kb` and Developer Zone at `ni.com/devzone` for more updated troubleshooting tips and answers to frequently asked questions about M Series devices.

D

Upgrading from E Series to M Series

The following KnowledgeBase and Developer Zone documents will help you overcome typical hurdles in upgrading from E Series to M Series devices.

- *Major Differences Between E Series and M Series DAQ Devices* KnowledgeBase lists the advantages of M Series over E Series and the functional differences and other differences between the two DAQ device families. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rdmess`.
- *Migrating an Application from E Series to M Series* Developer Zone document highlights the main differences to remember when moving an application from E Series to M Series devices. To access this document, go to `ni.com/info` and enter the info code `rde2m1`.
- *Using E Series Accessories with M Series Devices* KnowledgeBase describes how to use 68-pin E Series accessories with M Series devices. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rdea2m`.
- *M Series or S Series Devices Are Not Detected During Installation on Some Computers* KnowledgeBase describes the difference between M Series and E Series power rails, and the PCI specification for the PCI bus and power rails, and contains an up-to-date list of computers with power rails that do not support M Series devices. To access this KnowledgeBase, go to `ni.com/info` and enter the info code `rdmseis`.

E

Technical Support and Professional Services

Visit the following sections of the award-winning National Instruments Web site at `ni.com` for technical support and professional services:

- **Support**—Technical support resources at `ni.com/support` include the following:
  - **Self-Help Technical Resources**—For answers and solutions, visit `ni.com/support` for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at `ni.com/forums`. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support as well as exclusive access to on demand training modules via the Services Resource Center. NI offers complementary membership for a full year after purchase, after which you may renew to continue your benefits.

    For information about other technical support options in your area, visit `ni.com/services`, or contact your local office at `ni.com/contact`.
- **Training and Certification**—Visit `ni.com/training` for self-paced training, eLearning virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit `ni.com/alliance`.

- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electronic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`.
- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at `ni.com/calibration`.

If you searched `ni.com` and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

Glossary

Symbol	Prefix	Value
p	pico	10^{-12}
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Symbols

%	Percent.
+	Positive of, or plus.
–	Negative of, or minus.
±	Plus or minus.
<	Less than.
>	Greater than.
≤	Less than or equal to.
≥	Greater than or equal to.
/	Per.
º	Degree.
Ω	Ohm.

A

A	Amperes—the unit of electric current.
A/D	Analog-to-Digital. Most often used as A/D converter.
AC	Alternating current.
accuracy	A measure of the capability of an instrument or sensor to faithfully indicate the value of the measured signal. This term is not related to resolution; however, the accuracy level can never be better than the resolution of the instrument.
ADE	Application development environment.
AI	1. Analog input. 2. Analog input channel signal.
AI GND	Analog input ground signal.
AI SENSE	Analog input sense signal.
analog	A signal whose amplitude can have a continuous range of values.
analog input signal	An input signal that varies smoothly over a continuous range of values, rather than in discrete steps.
analog output signal	An output signal that varies smoothly over a continuous range of values, rather than in discrete steps.
analog signal	A signal representing a variable that can be observed and represented continuously.
analog trigger	A trigger that occurs at a user-selected point on an incoming analog signal. Triggering can be set to occur at a specific level on either an increasing or a decreasing signal (positive or negative slope). Analog triggering can be implemented either in software or in hardware. When implemented in software (LabVIEW), all data is collected, transferred into system memory, and analyzed for the trigger condition. When analog triggering is implemented in hardware, no data is transferred to system memory until the trigger condition has occurred.
AO	Analog output.

AO 0	Analog channel 0 output signal.
AO 1	Analog channel 1 output signal.
AO 2	Analog channel 2 output signal.
AO 3	Analog channel 3 output signal.
AO GND	Analog output ground signal.
application	A software program that creates an end-user function.
arm	The process of getting an instrument ready to perform a function. For example, the trigger circuitry of a digitizer is armed, meaning that it is ready to start acquiring data when an appropriate trigger condition is met.
ASIC	Application-specific integrated circuit—A proprietary semiconductor component designed and manufactured to perform a set of specific functions for a specific customer.
asynchronous	1. Hardware—A property of an event that occurs at an arbitrary time, without synchronization to a reference clock. 2. Software—A property of a function that begins an operation and returns prior to the completion or termination of the operation.

B

b	Bit—One binary digit, either 0 or 1.
B	Byte—Eight related bits of data, an eight-bit binary number. Also used to denote the amount of memory required to store one byte of data.
block diagram	A pictorial description or representation of a program or algorithm.
BNC	Bayonet-Neill-Concelman—A type of coaxial connector used in situations requiring shielded cable for signal connections and/or controlled impedance applications.
buffer	1. Temporary storage for acquired or generated data. 2. A memory device that stores intermediate data between two devices.

bus, buses — The group of electrical conductors that interconnect individual circuitry in a computer. Typically, a bus is the expansion vehicle to which I/O or other devices are connected. Examples of PC buses are the PCI, AT(ISA), and EISA bus.

C

C — Celsius.

calibration — The process of determining the accuracy of an instrument. In a formal sense, calibration establishes the relationship of an instrument's measurement to the value provided by a standard. When that relationship is known, the instrument may then be adjusted (calibrated) for best accuracy.

calibrator — A precise, traceable signal source used to calibrate instruments.

cascading — Process of extending the counting range of a counter chip by connecting to the next higher counter.

CE — European emissions control standard.

channel — Pin or wire lead to which you apply or from which you read the analog or digital signal. Analog signals can be single-ended or differential. For digital signals, you group channels to form ports. Ports usually consist of either four or eight digital channels.

clock — Hardware component that controls timing for reading from or writing to groups.

CMOS — Complementary metal-oxide semiconductor.

CMRR — Common-mode rejection ratio—A measure of the ability of a differential amplifier to reject interference from a common-mode signal, usually expressed in decibels (dB).

common-mode rejection — The ability of an electronic system to cancel any electronic noise pick-up that is common to both the positive and negative polarities of the input leads to the instrument front end. Common mode rejection is only a relevant specification for systems having a balanced or differential input.

common-mode signal
1. Any voltage present at the instrumentation amplifier inputs with respect to amplifier ground.
2. The signal, relative to the instrument chassis or computer's ground, of the signals from a differential input. This is often a noise signal, such as 50 or 60 Hz hum.

connector
1. A device that provides electrical connection.
2. A fixture (either male or female) attached to a cable or chassis for quickly making and breaking one or more circuits. A symbol that connects points on a flowchart.

convert rate
Reciprocal of the interchannel delay.

count
The number of events, such as zero crossings, pulses, or cycles.

counter
1. Software. A memory location used to store a count of certain occurrences.
2. Hardware. A circuit that counts events. When it refers to an instrument, it refers to a frequency counter.

counter/timer
A circuit that counts external pulses or clock pulses (timing).

D

D GND
Digital ground signal.

D-SUB connector
A serial connector.

DAC
Digital-to-Analog Converter—An electronic device, often an integrated circuit, that converts a digital number into a corresponding analog voltage or current.

In the instrumentation world, DACs can be used to generate arbitrary waveform shapes, defined by the software algorithm that computes the digital data pattern, which is fed to the DAC.

DAQ

1. Data acquisition—The process of collecting and measuring electrical signals from sensors, transducers, and test probes or fixtures and inputting them to a computer for processing.
2. Data acquisition—The process of collecting and measuring the same kinds of electrical signals with A/D and/or DIO devices plugged into a computer, and possibly generating control signals with D/A and/or DIO devices in the same computer.

DAQ device

A device that acquires or generates data and can contain multiple channels and conversion devices. DAQ devices include plug-in devices, PCMCIA cards, and DAQPad devices, which connect to a computer USB or 1394 (FireWire®) port. SCXI modules are considered DAQ devices.

DAQ-STC2

Data acquisition system timing controller chip.

data acquisition

The general concept of acquiring data, as in *begin data acquisition* or *data acquisition and control*. *See also* DAQ.

data transfer

A technique for moving digital data from one system to another.

Options for data transfer are DMA, interrupt, and programmed I/O. For programmed I/O transfers, the CPU in the PC reads data from the DAQ device whenever the CPU receives a software signal to acquire a single data point. Interrupt-based data transfers occur when the DAQ device sends an interrupt to the CPU, telling the CPU to read the acquired data from the DAQ device. DMA transfers use a DMA controller, instead of the CPU, to move acquired data from the device into computer memory. Even though high-speed data transfers can occur with interrupt and programmed I/O transfers, they require the use of the CPU to transfer data. DMA transfers are able to acquire data at high speeds and keep the CPU free for performing other tasks at the same time.

dB

Decibel—The unit for expressing a logarithmic measure of the ratio of two signal levels: dB = 20log10 V1/V2, for signals in volts.

DC

Direct current—although the term speaks of current, many different types of DC measurements are made, including DC Voltage, DC current, and DC power.

device

An electronic board that performs general analog or digital I/O functions on one or multiple channels, connected to a PC through a bus or I/O port, such as PCI, PXI, Ethernet, USB, or serial.

DIFF — Differential mode—An analog input mode consisting of two terminals, both of which are isolated from computer ground, whose difference is measured.

differential input — An input circuit that actively responds to the difference between two terminals, rather than the difference between one terminal and ground. Often associated with balanced input circuitry, but also may be used with an unbalanced source.

digital I/O — The capability of an instrument to generate and acquire digital signals.

Static digital I/O refers to signals where the values are set and held, or rarely change. Dynamic digital I/O refers to digital systems where the signals are continuously changing, often at multi-MHz clock rates.

digital signal — A representation of information by a set of discrete values according to a prescribed law. These values are represented by numbers.

digital trigger — A TTL level signal having two discrete levels—A high and a low level.

DIO — Digital input/output.

DMA — Direct Memory Access—A method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.

DMA controller chip — Performs the transfers between memory and I/O devices independently of the CPU.

driver — Software unique to the device or type of device, and includes the set of commands the device accepts.

E

E Series — A standard architecture for instrumentation-class, multichannel data acquisition devices.

edge detection — A technique that locates an edge of an analog signal, such as the edge of a square wave.

EEPROM — Electrically Erasable Programmable Read-Only Memory—ROM that can be erased with an electrical signal and reprogrammed. Some SCXI modules contain an EEPROM to store measurement-correction coefficients.

encoder — A device that converts linear or rotary displacement into digital or pulse signals. The most popular type of encoder is the optical encoder, which uses a rotating disk with alternating opaque areas, a light source, and a photodetector.

EXTCLK — External clock signal.

external trigger — A voltage pulse from an external source that causes a DAQ operation to begin.

EXTREF — External reference signal.

F

FIFO — First-In-First-Out memory buffer—A data buffering technique that functions like a shift register where the oldest values (first in) come out first. Many DAQ products and instruments use FIFOs to buffer digital data from an A/D converter, or to buffer the data before or after bus transmission.

The first data stored is the first data sent to the acceptor. FIFOs are often used on DAQ devices to temporarily store incoming or outgoing data until that data can be retrieved or output. For example, an analog input FIFO stores the results of A/D conversions until the data can be retrieved into system memory, a process that requires the servicing of interrupts and often the programming of the DMA controller. This process can take several milliseconds in some cases. During this time, data accumulates in the FIFO for future retrieval. With a larger FIFO, longer latencies can be tolerated. In the case of analog output, a FIFO permits faster update rates, because the waveform data can be stored on the FIFO ahead of time. This again reduces the effect of latencies associated with getting the data from system memory to the DAQ device.

filter — A physical device or digital algorithm that selectively removes noise from a signal, or emphasizes certain frequency ranges and de-emphasizes others. Electronic filters include lowpass, band-pass, and highpass types. Digital filters can operate on numeric data to perform equivalent operations on digitized analog data or to enhance video images.

filtering — A type of signal conditioning that allows you to filter unwanted frequency components from the signal you are trying to measure.

floating — The condition where a common mode voltage exists, or may exist, between earth ground and the instrument or circuit of interest. Neither the high, nor the low side of a circuit is at earth potential.

floating signal sources — Signal sources with voltage signals that are not connected to an absolute reference of system ground. Also called non-referenced signal sources. Some common examples of floating signal sources are batteries, transformers, and thermocouples.

FREQ OUT — Frequency Output signal.

frequency — The number of alternating signals that occur per unit time.

ft — Feet.

function
1. A built-in execution element, comparable to an operator, function, or statement in a conventional language.
2. A set of software instructions executed by a single line of code that may have input and/or output parameters and returns a value when executed.

G

glitch — An unwanted signal excursion of short duration that is usually unavoidable.

GND — *See* ground.

ground
1. A pin.
2. An electrically neutral wire that has the same potential as the surrounding earth. Normally, a noncurrent-carrying circuit intended for safety.
3. A common reference point for an electrical system.

H

hardware — The physical components of a computer system, such as the circuit boards, plug-in devices, chassis, enclosures, peripherals, and cables.

hardware triggering — A form of triggering where you set the start time of an acquisition and gather data at a known position in time relative to a trigger signal.

Hz

1. Hertz—The SI unit for measurement of frequency. One hertz (Hz) equals one cycle per second.
2. The number of scans read or updates written per second.

hysteresis

Lag between making a change and the effect of the change.

I

I/O

Input/Output—The transfer of data to/from a computer system involving communications channels, operator interface devices, and/or data acquisition and control interfaces.

impedance

1. The electrical characteristic of a circuit expressed in ohms and/or capacitance/inductance.
2. Resistance.

in.

Inch or inches.

instrument driver

A set of high-level software functions that controls a specific GPIB, VXI, or RS232 programmable instrument or a specific plug-in DAQ device. Instrument drivers are available in several forms, ranging from a function callable language to a virtual instrument (VI) in LabVIEW.

instrumentation amplifier

A circuit whose output voltage with respect to ground is proportional to the difference between the voltages at its two inputs. An instrumentation amplifier normally has high-impedance differential inputs and high common-mode rejection.

interchannel delay

Amount of time that passes between sampling consecutive channels in an AI scan list. The interchannel delay must be short enough to allow sampling of all the channels in the channel list, within the sample interval. The greater the interchannel delay, the more time the PGIA is allowed to settle before the next channel is sampled. The interchannel delay is regulated by ai/ConvertClock.

interface

Connection between one or more of the following: hardware, software, and the user. For example, hardware interfaces connect two other pieces of hardware.

interrupt, interrupt request line

1. A means for a device to notify another device that an event occurred.
2. A computer signal indicating that the CPU should suspend its current task to service a designated activity.

I_{OH}	Current, output high.
I_{OL}	Current, output low.
IRQ	*See* interrupt, interrupt request line.

K

kHz	Kilohertz—A unit of frequency; 1 kHz = 10^3 = 1,000 Hz.
kS	1,000 samples.

L

LabVIEW	A graphical programming language.
LED	Light-Emitting Diode—A semiconductor light source.
lowpass filter	A filter that passes signals below a cutoff frequency while blocking signals above that frequency.
LSB	Least Significant Bit.

M

m	Meter.
M Series	An architecture for instrumentation-class, multichannel data acquisition devices based on the earlier E Series architecture with added new features.
mass termination	USB or DAQPad devices where all signals flow through 68-pin connectors, as opposed to screw terminal or BNC variants.
measurement	The quantitative determination of a physical characteristic. In practice, measurement is the conversion of a physical quantity or observation to a domain where a human being or computer can determine the value.
measurement device	DAQ devices, such as the M Series multifunction I/O (MIO) devices, SCXI signal conditioning modules, and switch modules.
MHz	Megahertz—A unit of frequency; 1 MHz = 10^6 Hz = 1,000,000 Hz.

micro (μ) — The numerical prefix designating 10^{-6}.

MIO — Multifunction I/O—DAQ module. Designates a family of data acquisition products that have multiple analog input channels, digital I/O channels, timing, and optionally, analog output channels. An MIO product can be considered a miniature mixed signal tester, due to its broad range of signal types and flexibility. Also known as multifunction DAQ.

MITE — MXI Interface To Everything—A custom ASIC designed by National Instruments that implements the PCI bus interface. The MITE supports bus mastering for high-speed data transfers over the PCI bus.

module — A board assembly and its associated mechanical parts, front panel, optional shields, and so on. A module contains everything required to occupy one or more slots in a mainframe. SCXI and PXI devices are modules.

monotonicity — A characteristic of a DAC in which the analog output always increases as the values of the digital code input to it increase.

multichannel — Pertaining to a radio-communication system that operates on more than one channel at the same time. The individual channels might contain identical information, or they might contain different signals.

multifunction DAQ — *See* MIO.

multiplex — To assign more than one signal to a channel. *See also* mux.

mux — Multiplexer—A set of semiconductor or electromechanical switches arranged to select one of many inputs to a single output. The majority of DAQ cards have a multiplexer on the input, which permits the selection of one of many channels at a time.

A switching device with multiple inputs that sequentially connects each of its inputs to its output, typically at high speeds, in order to measure several signals with a single analog input channel.

N

NI — National Instruments.

NI-DAQ — The driver software needed to use National Instruments DAQ devices and SCXI components. Some devices use Traditional NI-DAQ (Legacy); others use NI-DAQmx.

NI-DAQmx — The latest NI-DAQ driver with new VIs, functions, and development tools for controlling measurement devices. The advantages of NI-DAQmx over earlier versions of NI-DAQ include the DAQ Assistant for configuring channels and measurement tasks for your device for use in LabVIEW, LabWindows/CVI, and Measurement Studio; increased performance such as faster single-point analog I/O; and a simpler API for creating DAQ applications using fewer functions and VIs than earlier versions of NI-DAQ.

NI-PGIA — *See* instrumentation amplifier.

non-referenced signal sources — Signal sources with voltage signals that are not connected to an absolute reference or system ground. Also called floating signal sources. Some common example of non-referenced signal sources are batteries, transformers, or thermocouples.

NRSE — Non-Referenced Single-Ended mode—All measurements are made with respect to a common (NRSE) measurement system reference, but the voltage at this reference can vary with respect to the measurement system ground.

O

offset — The unwanted DC voltage due to amplifier offset voltages added to a signal.

P

PCI — Peripheral Component Interconnect—A high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It offers a theoretical maximum transfer rate of 132 MB/s.

PCI Express — A high-performance expansion bus architecture originally developed by Intel to replace PCI. PCI Express offers a theoretical maximum transfer rate that is dependent upon lane width. a ×1 link theoretically provides 250 MB/s in each direction—to and from the device. Once overhead is accounted for, a ×1 link can provide approximately 200 MB/s of input capability and 200 MB/s of output capability. Increasing the number of lanes in a link increases maximum throughput by approximately the same factor.

PCIe — *See* PCI Express.

period	The period of a signal, most often measured from one zero crossing to the next zero crossing of the same slope. The period of a signal is the reciprocal of its frequency (in Hz). Period is designated by the symbol T.
PFI	Programmable Function Interface.
PGIA	Programmable Gain Instrumentation Amplifier.
physical channel	*See* channel.
Plug and Play devices	A specification prepared by Microsoft, Intel, and other PC-related companies that result in PCs with plug-in devices that can be fully configured in software, without jumpers or switches on the devices.
posttriggering	The technique used on a DAQ device to acquire a programmed number of samples after trigger conditions are met.
power source	An instrument that provides one or more sources of AC or DC power. Also known as power supply.
ppm	Parts per million.
pretriggering	The technique used on a DAQ device to keep a continuous buffer filled with data, so that when the trigger conditions are met, the sample includes the data leading up to the trigger condition.
pulse	A signal whose amplitude deviates from zero for a short period of time.
pulse width	The time from the rising to the falling slope of a pulse (at 50% amplitude).
PXI	A rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXIbus standard was originally developed by National Instruments in 1997, and is now managed by the PXIbus Systems Alliance.
PXI Express	PCI Express eXtensions for Instrumentation—The PXI implementation of PCI Express, a scalable full-simplex serial bus standard that operates at 2.5 Gbps and offers both asynchronous and isochronous data transfers.

PXI_STAR — A special set of trigger lines in the PXI backplane for high-accuracy device synchronization with minimal latencies on each PXI slot. Only devices in the PXI Star controller Slot 2 can set signal on this line. For additional information concerning PXI star signal specifications and capabilities, read the PXI Specification located at `www.pxisa.org/specs`.

PXIe — *See* PXI Express.

Q

quadrature encoder — An encoding technique for a rotating device where two tracks of information are placed on the device, with the signals on the tracks offset by 90° from each other. This makes it possible to detect the direction of the motion.

R

range — The maximum and minimum parameters between which a sensor, instrument, or device operates with a specified set of characteristics. This may be a voltage range or a frequency range.

real time

1. Displays as it comes in; no delays.
2. A property of an event or system in which data is processed and acted upon as it is acquired instead of being accumulated and processed at a later time.
3. Pertaining to the performance of a computation during the actual time that the related physical process transpires so results of the computation can be used in guiding the physical process.

RSE — Referenced Single-Ended configuration—All measurements are made with respect to a common reference measurement system or a ground. Also called a grounded measurement system.

RTSI — Real-Time System Integration.

RTSI bus — Real-Time System Integration bus—The National Instruments timing bus that connects DAQ devices directly, by means of connectors on top of the devices, for precise synchronization of functions.

S

s	Seconds.
S	Samples.
sample counter	The clock that counts the output of the channel clock, in other words, the number of samples taken. On devices with simultaneous sampling, this counter counts the output of the scan clock and hence the number of scans.
scan	One or more analog or digital input samples. Typically, the number of input samples in a scan is equal to the number of channels in the input group. For example, one pulse from the scan clock produces one scan which acquires one new sample from every analog input channel in the group.
scan interval	Controls how often a scan is initialized; is regulated by the AI Sample Clock signal.
scan rate	Reciprocal of the scan interval.
SCC	Signal Conditioning Carriers—A compact, modular form factor for signal conditioning modules.
SCXI	Signal Conditioning eXtensions for Instrumentation—The National Instruments product line for conditioning low-level signals within an external chassis near sensors so that only high-level signals are sent to DAQ devices in the noisy PC environment.
sensor	A device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on), and produces a corresponding electrical signal. Primary characteristics of sensors are sensitivity, frequency range, and linearity.
signal conditioning	1. Electronic equipment that makes transducer or other signals suitable in level and range to be transmitted over a distance, or to interface with voltage input instruments. 2. The manipulation of signals to prepare them for digitizing.
signal source	A generic term for any instrument in the family of signal generators.
signals	Signals are waveforms containing information. Although physical signals can be in the form of mechanical, electromagnetic, or other forms, they are most often converted to electronic form for measurement.

single trigger mode — When the arbitrary waveform generator goes through the staging list only once.

single-buffered — Describes a device that acquires a specified number of samples from one or more channels and returns the data when the acquisition is complete.

single-ended input — A circuit that responds to the voltage on one input terminal and ground. *See also* differential input.

single-ended output — A circuit whose output signal is present between one output terminal and ground.

software applications — The programs that run on your computer and perform a specific user-oriented function, such as accounting, program development, measurement, or data acquisition. In contrast, operating system functions basically perform the generic "housekeeping" of the machine, which is independent of any specific application. Operating system functions include the saving of data (file system), handling of multiple programs at the same time (multi-tasking), network interconnection, printing, and keyboard/user interface interaction.

software triggering — A method of triggering in which you simulate an analog trigger using software. Also called *conditional retrieval*.

source impedance — A parameter of signal sources that reflects current-driving ability of voltage sources (lower is better) and the voltage-driving ability of current sources (higher is better).

synchronous

1. Hardware—A property of an event that is synchronized to a reference clock.
2. Software—A property of a function that begins an operation and returns only when the operation is complete. A synchronous process is, therefore, *locked* and no other processes can run during this time.

T

task — In NI-DAQmx, a collection of one or more channels, timing, and triggering and other properties that apply to the task itself. Conceptually, a task represents a measurement or generation you want to perform.

TC — *See* terminal count.

terminal	An object or region on a node through which data passes.
terminal count	The highest value of a counter.
t_{gh}	Gate hold time.
t_{gsu}	Gate setup time.
t_{gw}	Gate pulse width.
Timebase	The reference signals for controlling the basic accuracy of time or frequency-based measurements. For instruments, timebase refers to the accuracy of the internal clock.
t_{out}	Output delay time.
Traditional NI-DAQ (Legacy)	An upgrade to the earlier version of NI-DAQ. Traditional NI-DAQ (Legacy) has the same VIs and functions and works the same way as NI-DAQ 6.9.*x*. You can use both Traditional NI-DAQ (Legacy) and NI-DAQmx on the same computer, which is not possible with NI-DAQ 6.9.*x*.
transducer	A device that responds to a physical stimulus (heat, light, sound, pressure, motion, flow, and so on), and produces a corresponding electrical signal. *See also* sensor.
trigger	1. Any event that causes or starts some form of data capture. 2. An external stimulus that initiates one or more instrument functions. Trigger stimuli include a front panel button, an external input voltage pulse, or a bus trigger command. The trigger may also be derived from attributes of the actual signal to be acquired, such as the level and slope of the signal.
t_{sc}	Source clock period.
t_{sp}	Source pulse width.
TTL	Transistor-Transistor Logic—A digital circuit composed of bipolar transistors wired in a certain manner. A typical medium-speed digital technology. Nominal TTL logic levels are 0 and 5 V.

U

USB — Universal Serial Bus—A 480 Mbit/s serial bus with up to 12-Mbps bandwidth for connecting computers to keyboards, printers, and other peripheral devices. USB 2.0 retains compatibility with the original USB specification.

V

V — Volts.

V_{cm} — Common-mode voltage.

V_g — Ground loop voltage.

V_{IH} — Volts, input high.

V_{IL} — Volts, input low.

V_{in} — Volts in.

V_m — Measured voltage.

V_{OH} — Volts, output high.

V_{OL} — Volts, output low.

V_{out} — Volts out.

V_s — Signal source voltage.

virtual channel — *See* channel.

W

waveform

1. The plot of the instantaneous amplitude of a signal as a function of time.
2. Multiple voltage readings taken at a specific sampling rate.

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